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A 2D Analytical Model for Potential Distribution of GAA Tunnel Field Effect Transistor

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ABSTRACT

The effect of binary metal gate alloy on the surface potential of nanoscale gate all around TFET has been studied. Binary metal alloy gate consists of two gate metals with different work functions. A two dimensional analytical model has been developed for the tunnel FET designed using binary metal alloy gate and compared with the existing models and simulation work. Different binary metal alloy gates were also studied and compared in this study.

Keywords: Binary metal alloy, GAA, TFET

1. INTRODUCTION

The presence of very large number of analog and digital devices in an IC chip which comprises millions of transistor that causes major and significant power dissipation. So when we move towards lower feature size of device (Device Downscaling) then power dissipation becomes more and this is important factor to investigate. TFET device has some advantages like low subthreshold swing, steep slope, low off current (I_{OFF}), fast switching action, immunity against temperature variation and most important low energy consumption. Moreover, this device (TFET) has some limitations like low on current compare to MOSFET device, am-bipolar conduction and high gate to drain capacitance that causes several undesirable effect on device performance.

To overcome these problems several architectures and models have been proposed some of them are listed as Group III-V semiconductor based TFET, Carbon based TFET, Hetero-dielectric based TFET, Homo-junction TFET, Hetero-junction TFET, DMG (Double Metal Gate) TFET, Binary Alloy GAA TFET [1-3]. Power dissipation problem can be reduced through reducing the off state current (I_{OFF}) and subthreshold swing (SS) of device [4-6]. Concept of DMG fails for shorter length device due to fabrication difficulty and gate alignment problem.

Alternative structure called BMA (Binary Metal Alloy) with single gate have been proposed to overcome these issues. BMA comprises two different metal having different work function. At source end there is lesser work function compared to drain end but this is linearly graded work function [7]. This new composition of two metal makes alloy which has similar function as Double Metal Gate (DMG) do. So new structure has been proposed having single gate (SG) to work same as Dual Metal Gate (DMG) [8-9]. The advantage of this structure (Single Gate) over DMG is that SG can easily be fabricated and there is no need of gate alignment. Recently new TFET model have been proposed name as GAA TFET with Binary Metal Alloy (BMA) Gate [10]. To study the behavior of TFET [11-12] several analytical models have been developed. GAA gate TFET having special characteristics length due to this it provides optimum scaling capability of device [13-16].

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In this paper we have made an attempt to study the modeling methodology of GAA TFET with Binary Metal Alloy (BMA) Gate and the benefits of BMA over conventional architecture(CCT). Binary Metal Alloy provides larger tunneling distance when the device is in off state i.e. at $V_G = 0V$, as a result subthreshold swing reduces below 40 mV/decade. We have proposed model for surface potential and compared it with reported data[10]. The key steps regarding the modeling approach has been discussed in the next section.

2. DEVICE STRUCTURE

In present work n-type GAA TFET architecture with binary alloy composition in the metal gate has been considered and shown in figure 1. The doping concentration for source as well as drain region is kept equal to 10^{20} cm^{-3} respectively. The channel region is made up of intrinsic Silicon which is lightly doped of the order of 10^{15} cm^{-3}. The thickness of the oxide layer (tox) and silicon body diameter (tsi) are 2 nm and 10 nm, respectively. The length of channel (Lc) and source/drain (Ls/Ld) regions and are taken as 50nm and 20nm respectively.

In this present model, $Ta_kPt_{1\text{-}k}$ has been considered as the gate material. Here k value lies between $(0 \leq k \leq 1)$. The gate metal *Ta* and *Pt* have been considered with different work function values of 4.2 eV and 5 eV respectively and linear grading of the junction has been done.

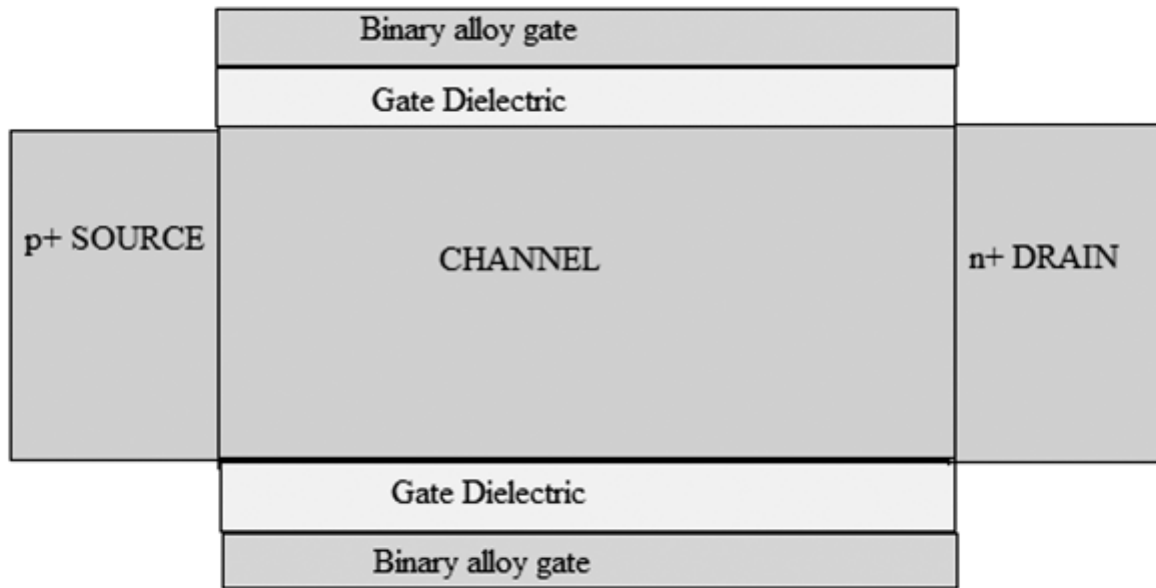

Figure1: Device architecture for Binary Metal Alloy (BMA) GAA Gate Tunnel FET

3. MODEL FORMULATION

Two dimensional Poisson's equation can be solved to obtain the potential profile along the channel. To solve the Poisson's equation, we used parabolic approximation [17] method. The 2-D Poisson's equation in the cylindrical co-ordinate is expressed as:

$$\frac{1}{r}\frac{d}{dr}\left(r*\frac{d}{dr}\phi(r,z)+\frac{d^2}{dz^2}\phi(r,z)=\frac{q*Nc}{\varepsilon_{si}}\right) \tag{1}$$

Where the doping concentration of Silicon body is Nc, $\varphi(r, z)$ is the electrostatic potential in the intrinsic channel region, $\in_{si}$ is the dielectric permittivity of silicon.

The potential profile along the channel region can be solved by using proper boundary conditions (similar to [17]) and parabolic approximation given by

$$\phi(r,z) = a0(z) + r * al(z) + r^2 * a2(z) \tag{2}$$

The coefficients a0, a1, a2 of the polynomial equation are very important to find the solution of 2-D Laplace equation. So for that we are using boundary conditions: 1) The electrical flux between the silicon film and surrounding gate oxide must be continuous. 2) The electrical field at r = 0 must be zero due to the symmetry of the channel potential along the r direction. Hence the coefficients are obtained as:

$$\begin{aligned} &a0(z,VDS,VGS) \\ &= \phi_S(Z,VDS,VGS) \\ &- \frac{C_{ox} * t_{si} * (\phi_{GS}(z,VGS) - \phi_s(Z,VDS,VGS))}{4 * \varepsilon_{si}} \end{aligned} \tag{3}$$

$$a1(z,VGS) = 0 \tag{4}$$

$$a2(z,VDS,VGS) = \frac{C_{ox*}((z,VGS) - \phi_s(z,VDS,VGS))}{t_{si*\varepsilon_{si}}} \tag{5}$$

After getting the coefficients a0, a1, a2 we put the values of these coefficients in the equation (2) and then we find the potential profile ϕ(r, z). Now differentiating and double differentiating ϕ(r, z) and putting this value in equation (1), we get the one dimensional Poisson's equation as:

$$\frac{d^2}{dz^2}\phi_s(z) + \frac{VGS - (\psi_{mi}(z) - \psi_{si}(z)) - \phi_s(z)}{\lambda^2} = \frac{q * Nc}{\varepsilon_{si}} \tag{6}$$

Where $\phi_s(z)$ represents the potential profile at the gate oxide channel interface ($r = \pm t_{si}/2$). Similarly, V_{GS} is the voltage applied at the gate terminal and ε_{si} is the dielectric constant of silicon. The flat-band voltage (V_{FBi}) at any point in the channel is evaluated using the instantaneous work-function of the alloy ($\psi_{mi}(z)$) and work-function of silicon (ψ_{si}). λ is known as the characteristic length of the cylindrical gate and is mathematically expressed as

$$\lambda = \sqrt{\frac{t_{si^2} * \varepsilon_{si} * \ln\left(1 + \frac{2 * t_{ox}}{t_{si}}\right)}{8 *_{ox}}} \tag{7}$$

Where the various terms are already mentioned

To find the potential profile we use the boundary conditions at the source channel and drain channel interface. These boundary conditions for the realization of surface potential are

$$\phi_s(z)|_{z=0} = V_{bis}$$

$$\phi_s(z)|_{z=Lc} = V_{bid}$$

Where V_{bis} and V_{bid} are known as built-in-potential in the source and drain interface respectively. After doing so we get the differential equation as:

$$\frac{d^2}{dz^2}\phi_s(Z) - \frac{4 * C_{ox}}{\varepsilon_{si*}t_{si}}\phi_s(z) = C \tag{8}$$

Where “C” is the constant term and can be expressed as,

$$C = \frac{q * Nc}{\varepsilon_{si}} - \frac{4 * C_{ox}}{\varepsilon_{si*} t_{si}} \tag{9}$$

Now the differential equation (4) can be solved for the surface potential of the channel by using an auxiliary equation and we have some coefficients terms as Az (z, VDS, VGS), Bz (z, VDS, VGS) and $C_{mi.}$

$$\begin{aligned} \phi_{s(z,VDS,VGS)} &= A_z\left(y,VDS,VGS\right) * e^{\frac{z}{\lambda}} \\ &+ B_z\left(z,VDS,VGS\right) * e^{\frac{-z}{\lambda}} \\ &- C_{mi}\left(z,VGS\right) \end{aligned} \tag{10}$$

Where,

$$A_z\left(z,VDS,VGS\right) = \frac{\left(V_{bid}\left(VDS\right) + c_{mi}\left(z,VGS\right)\right) * e^{\frac{LC}{\lambda}} - \left(V_{bis} + C_{mi}\left(z,VGS\right)\right)}{e^{\frac{2*LC}{\lambda}} - 1} \tag{11}$$

$$B_z\left(z,VDS,VGS\right) = \frac{\left(V_{bid}\left(VDS\right) + c_{mi}\left(z,VGS\right)\right) * e^{\frac{-LC}{\lambda}} - \left(V_{bis} + C_{mi}\left(z,VGS\right)\right)}{e^{\frac{-2*LC}{\lambda}} - 1} \tag{12}$$

$$C_{mi}\left(z,VGS\right) = \psi_{mi}\left(z\right) - \psi_{si}\left(z\right) - VGS + \frac{q * Nc * \lambda^2}{\varepsilon_{si}} \tag{13}$$

The model derives above is very general and can be found as simple 2D analytical model for modelling semiconductor devices.

4. RESULTS AND DISCUSSION

The model derived above can be well used for work function engineered devices. The modeled results have been plotted for PtTi binary alloy and compared with the published data[10].

Figure 2 represents the surface potential variation along the channel direction with varying gate bias (V_{GS}) at fixed drain voltage value of 1.0 V. These results have been plotted for both the cases i.e. for the conventional GAA TFET (CCT) architecture and for GAA TFET with Binary Metal Alloy (BMA) Gate. It can be clearly observed that the potential profile for BMA TFETs is more or less similar to Dual Metal Gate TFETs having two metal gates at source (low work function) and drain (high work function) end respectively. This is because the work function of BMA is varying linearly along the channel since the composition of Metal B (Pt) in the alloy i.e. Ta_kPt_{k-1} is linearly varying [10]. It can be clearly observed that increasing the value of the gate voltage increases the potential in the channel region for both the architectures i.e. for CCT and for BMA TFETs.

Comparing both the architectures, it can be seen that the slope of potential for both the devices is more or less similar to each other and therefore would result in similar tunneling barrier width during the on-state and therefore it can be predicted that both the device architectures would result in almost similar on-state current (I_{ON}).

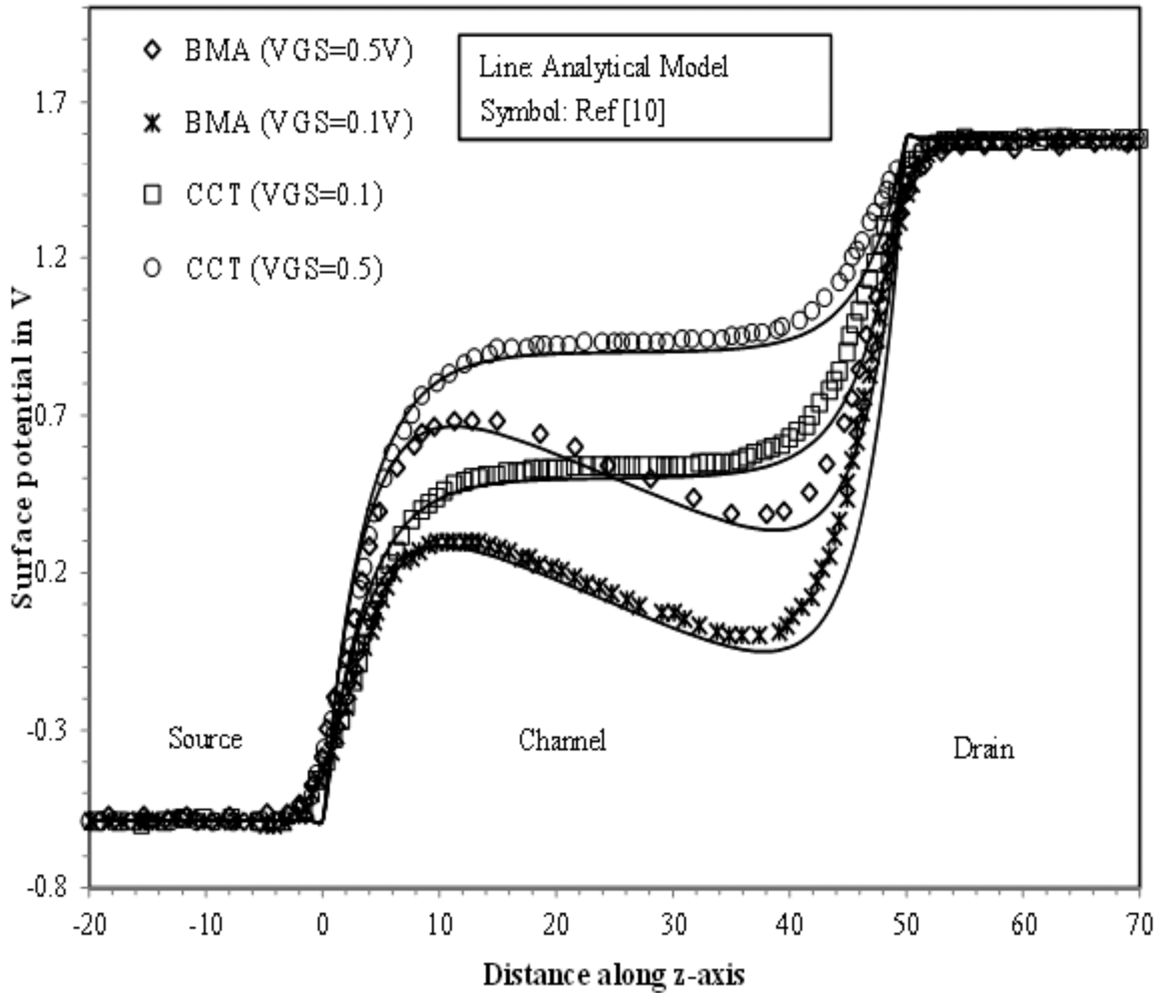

Figure 2: Surface potential along the channel at different Gate Voltages

Other binary alloys like TaTi, RuY, MoTa, RuTa, AlTa etc., which have work function in the range of 3.9eV to 5.1eV are suitable for gate electrode. A detailed work on binary metal alloys can be found in literature [20]. With device miniaturization and decreasing oxide thicknesses, the leakage current and stability issues can be largely reduced by choosing proper metal gat electrodes. Proper metal gates are responsible for eliminating dopant distribution effects and sheet resistance constraints. So work function tuning has become important in predicting potential profiles and subsequently other electrical parameters.

Figure 3 represents the potential variation along the channel region at varying drain voltage (VDS) values of 0.1 and 1 V respectively and at fixed gate voltage (VGS) value of 0.1V. The variation in the drain voltage can be clearly seen from the figure at drain channel junction. All the modeled results are showing good agreement with the published data [10].

Analysis has been carried out with other variants of binary alloys and surface potential has more or less the same trend.

5. CONCLUSION

In this paper a simple analytical model is developed forGAA TFET with BMA gate.The curves for potential with gate and drain voltage variation have been plotted. For proper validation or our modeled data a comparison with published data has been done. All the modeled results are in good agreement. The work can further be extended to obtain the electrical characteristics of the device.

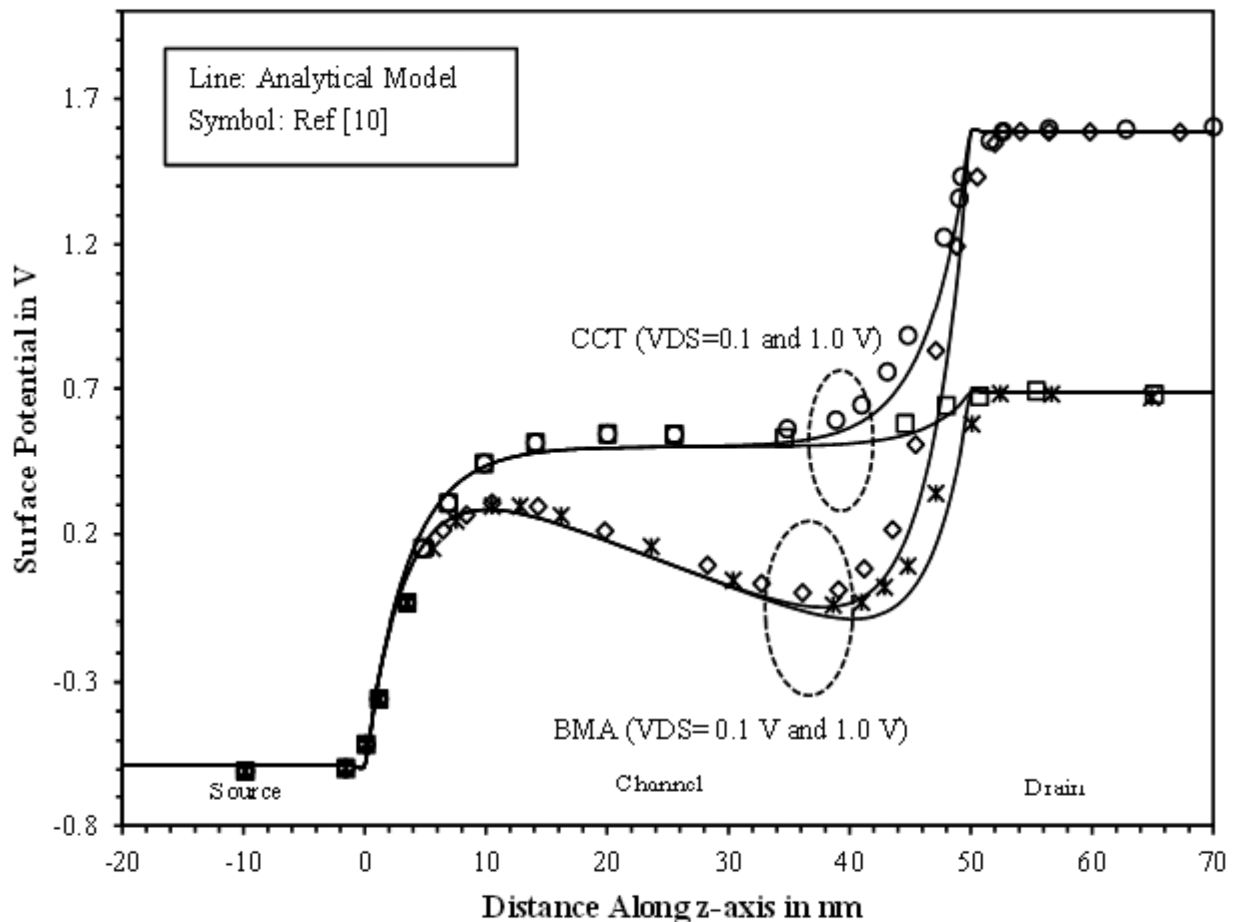

Figure 3: Surface Potential along the channel at different Drain Voltages

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