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A NOVEL DESIGN AND IMPLEMENTATION OF BINARY TO GRAY CODE CONVERTERS UP TO 4-BIT BY QUANTUM DOT CELLULAR AUTOMATA

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Abstract: Quantum-dot Cellular Automata (QCA) are dominant nanotechnology which has been utilized widely in computerized circuits and frameworks. It is a promising other option to complementary metal–oxide–semiconductor (CMOS) innovation with many luring components, for example, rapid, low control utilization and higher exchanging recurrence than transistor based innovation. The code converters are the essential unit for change of information to execute arithmetic processes. In this paper, QCA based 2-bit binary-to-gray; 3-bit binary-to-gray and 4-bit binary-to-gray code converter have been proposed. The proposed configuration decreases the numbers of cells, area, and raises exchanging speed. The simulations are completed using QCA Designer. We have performed a comparative study of proposed design with recent designs and proved that proposed design is broadly utilized for simulation and confirmation.

Key Words: *Binary to Gray Converter; Quantum Dot Cellular Automata; Gray Code; QCA cell.*

I. INTRODUCTION

QCA is an advanced access towards the modern era of nanotechnology and an option of CMOS innovation [1] and offers another new designing strategy which is applicable for logic gates. Physical limits of CMOS, for example, quantum impacts and mechanical points of confinement like power scattering; hamper the energy of microelectronics utilizing customary circuit scaling [2]. QCA is a rising innovation which permits working frequencies in the scope of THz [3] that is most certainly not achievable in current CMOS advance. Conversation circuit inserted between two structures if every utilizations diverse codes for a similar data. A code converter is a combinational circuit which generates two structures reliable even every utilizations particular binary code. n this paper, we have planned and executed a 2-bit binary-to-gray, 3-bit binary-to-gray and 4-bit binary-to-gray code converter in QCA innovation. We actualize the binary-to-gray converter in a proficient way utilizing less a number of cell and zone.

Fundamentals of QCA –

The main unit of QCA structure is QCA cell and it comprises of two electrons with four quantum dots situated at the vertices of a squared cell [4-6]. Electrons can move to various quantum dots by a method for electron tunneling. The electrons are forced to the corner zone to grow their division due to Coulomb repugnance. The state of a cell is called its polarization. The identical energetically ostensible plans of the two electrons in the QCA cell, as appeared in Figure 1. These two stable arrangements of electrons are signified as cell polarization P= + 1.00 and P = –

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1.00. By utilizing cell polarization P = + 1.00 to represents rationale "1" and P = –1.00 to represents rationale "0", binary
Information is encoded in the charge composition of the QCA cell [7, 8].

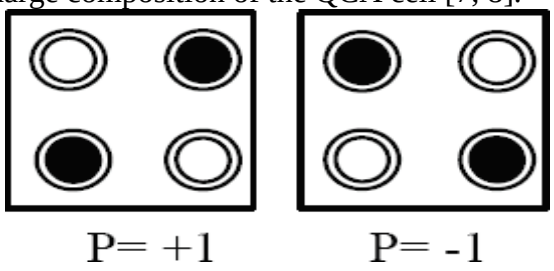


Figure 1. Structure of a basic QCA cell

Various QCA combinational [1, 5, 9-22], consecutive [23-32] and reversible logic [33-40] circuit have been proposed in recent years based on two cell inverters and three input majority voter element [10, 17, 41, 42]. Elemental structures for QCA are the inverter and the majority gate. The element blocks of QCA logic include a QCA wire, QCA inverter and QCA majority gate.

QCA Wire –

QCA wire is a heap of interconnecting cells that are utilized to exchange polarization state. QCA wire can be comprised of 45^o cells or 90^o cells appeared in figure 2 respectively. The formal arrangement of QCA cells designs a binary wire. For the electrostatic interchanges between the cells the signal propagates from one end then onto the next. For a 45^o QCA wire the engendering of the signal must be exchanged between the two polarizations [43].

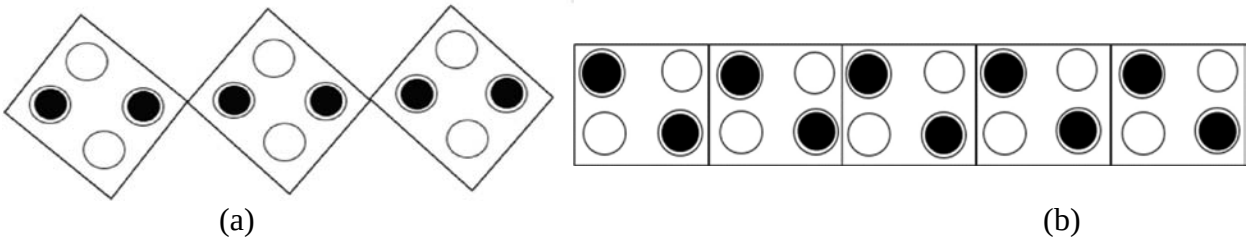


Figure 2. QCA (a) 45° wire (b) 90° wire.

QCA inverter –

QCA inverter is generally composed by placing the cells with only their edges contacts. This aspect is employed to forge an inverter as shown in Figure 3. QCA inverter returns the reversed value of the input value.

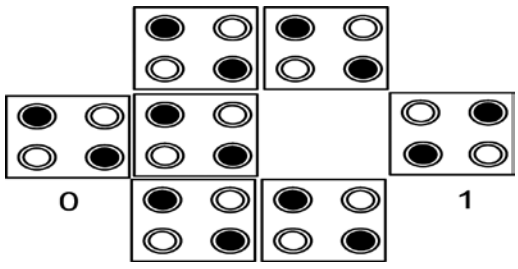


Figure 3 . QCA inverter

Majority voter (MV) –

The MV has four terminal cells. Among these terminals three are characterizing as input terminal cells and resting one characterizing as output cell .Majority Gate [44] is communicated as logical function.MV (A, B, C) = AB + BC + AC. To deliver efficient QCA design, the digital circuits are executed with the assistance of majority, gate-based procedures are required [45].Logical AND gate and OR gate can be can be acknowledged from majority gate as shown in Figure 4.

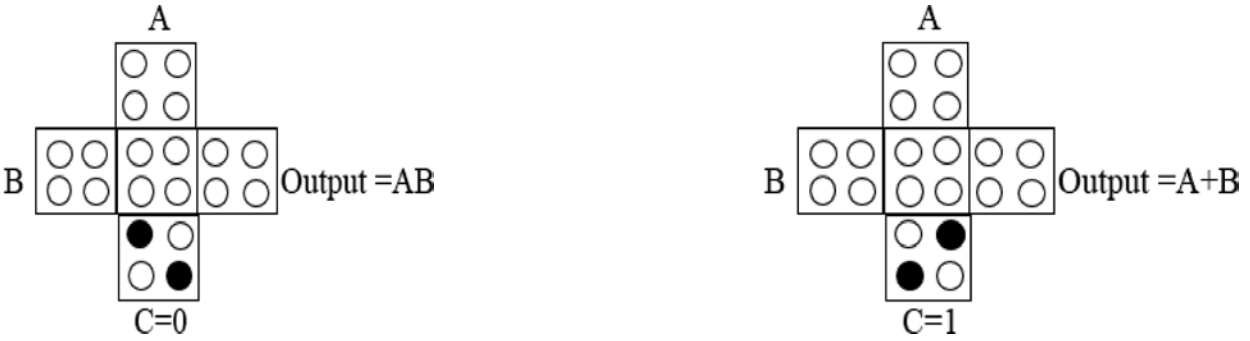


Figure 4. 2-input AND gate and 2-input OR gate using Majority voter

QCA Clocking–

The clocking of QCA can be refined by controlling the potential barriers between adjacent quantum-dots. At the point when the potential is low the electron wave capacities get to be delocalized bringing about no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell tends to gain a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched . Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each $\pi/2$ degrees out of phase is all that is required by any QCA circuit as shown in Figure 5[46].

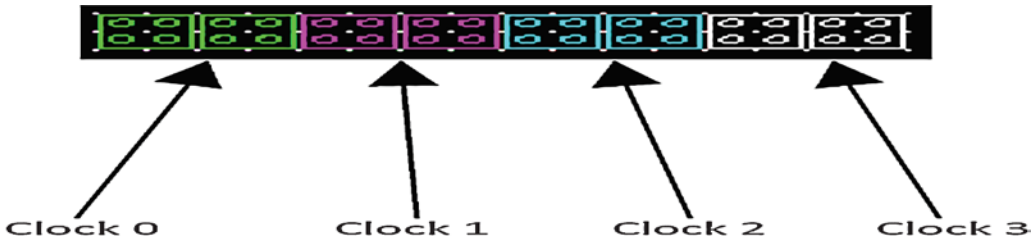


Figure 5. QCA clocking.

II. PROPOSED ALGORITHM

2.1 Methodology –

QCA calculation continues by direction of cells based on of polarization of connecting cells. An investigation is executed to discover the proper instruments and check the proposed circuit. A few inexact test systems as nonlinear estimation procedures and bit stable engine are used to illustrate. These methods don't create the bona fide divide. At that point, QCA Designer 2.0.3 is favored and this reproduction engine is portrayed [47]. QCA Designer is an apparatus utilized for model and reproduction of QCA based circuit advanced at the ATIPS Laboratory. The usefulness of the circuit is tried by QCA Designer 2.0.3 [48] which includes default values, for example,

cell measure, a number of tests, the range of impact, meeting resistance, relative permittivity, clock plenty fullness figure, Relaxation time and so forth. For executing the code converter in CMOS we utilized MICROWIND [49] which is an incorporated instrument for recreation.

2.2 Proposed Circuit and Presentation –

The massive accessibility of codes for comparing diverse components of data results in the utilization of unmistakable codes by particular plans and it is required some of the time to utilize the consequence of the one framework as utilized to the contribution to another framework. Code converters are circuits that change over a code into another which is logical arrays and utilized as a part of many fields, for example, shielding data from outsiders and increment information adaptability. It is likewise effective in security division for concocting and figuring out codes.

2.3 Binary code –

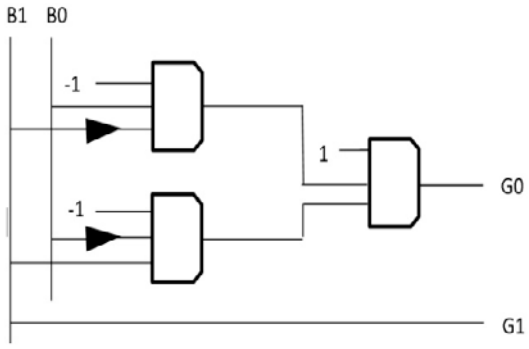
A code is a symbolic presentation of data and performs text information using the number system. For instance a binary sequence of six bits 110100 is identical to decimal number 52.

2.4 *Gray code –*

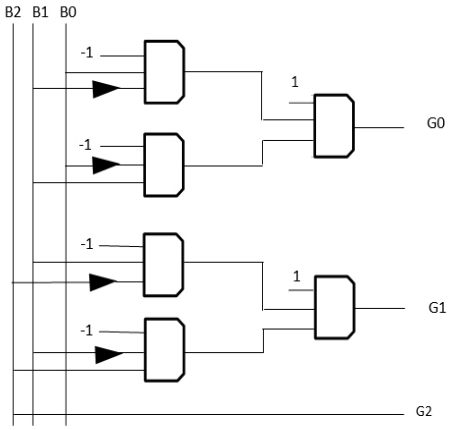
Reflected binary code, also known as Gray code is a numeral structure where each value differs only a sole bit from the previous bit. Gray code is not convenient for arithmetic operations. Gray code has many constructive applications including simplify fault correction, terrestrial television, some cable television system, analog-to-digital converter and peripheral apparatus.

2.5 QCA Implementation of Code Converters –

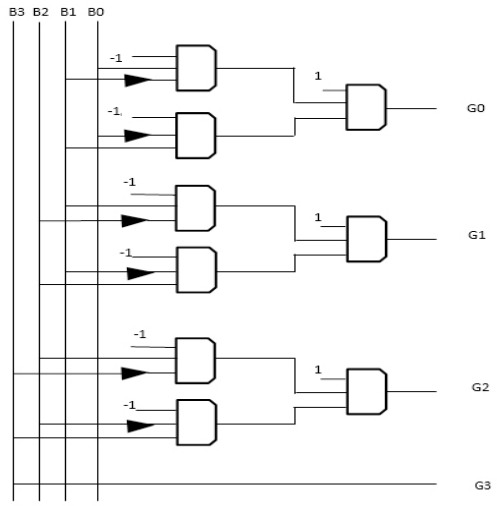
In Figure.6 shows the simplified block diagram of 2-bit binary-to-gray, 3-bit binary-to-gray and 4-bit binary-to-gray code converter using majority voter.



(a)



(b)



(c)

Figure 6. Block diagram of (a) 2-bit binary-to-gray (b) 3-bit binary-to-gray (c) 4-bit binary-to-gray code converter.

A two bit binary-to-gray code converter composed of two binary inputs B1 and B0 and the corresponding gray outputs are G1 and G0. Three bit binary-to-gray code converter composed of 3-inputs B0, B1 and B2 and the corresponding gray outputs are G0, G1 and G2. Four bit binary-to-gray code converter composed of 4-inputs B3, B2, B1 and B0 and the corresponding gray outputs are G3, G2, G1 and G0. Tables 1 to 3 show the truth table of binary-to-gray code converter.

Table -1 Truth table Representations of two bit Binary to Gray Code Converter.

Binary Inputs		Gray Outputs	
B1	B0	G1	G0
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table -2 Truth table Representations of three bit Binary to Gray Code Converter.

Binary Inputs			Gray Outputs		
B0	B1	B2	G0	G1	G2
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table -3 Truth table Representations of four bit Binary to Gray Code Converter.

Binary Inputs				Gray Outputs			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

2.6 Simulation and Result–

The code converter circuits are designed using QCA Designer 2.0.3. The simulated circuit layout of 2-bit binary to gray, 3-bit binary to gray and 4-bit binary to gray code converter are shown in figure 6 to 8 respectively. The object parameters: cell width × cell height is 18 × 18 and dot diameter is 5.00. The logical equation of two bit binary to gray code converter is G1 = B1 and G0 = B1⊕B0. For three bit binary to gray code converter the logical equation is G0 = B0, G1 = B1⊕B0 and G2 = B2⊕B1.The logical equation of four bit binary to gray code converter is G3 = B3, G2 = B3⊕B2, G1 = B2⊕B1 and G0 = B1⊕B0.

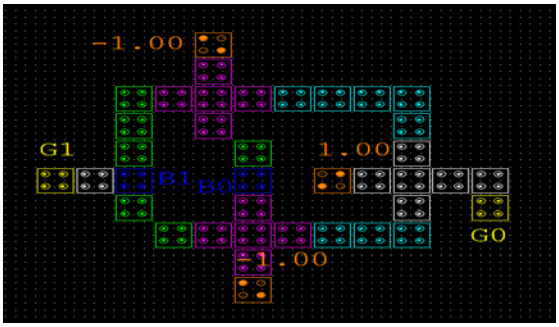


Figure 7. QCA implementation of two bit binary to gray code converter.

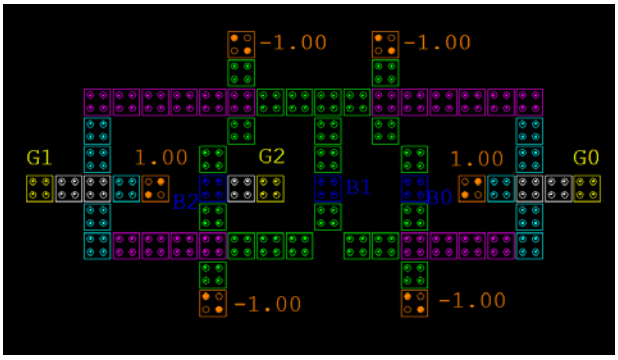


Figure 8. QCA implementation of three bit binary to gray code converter.

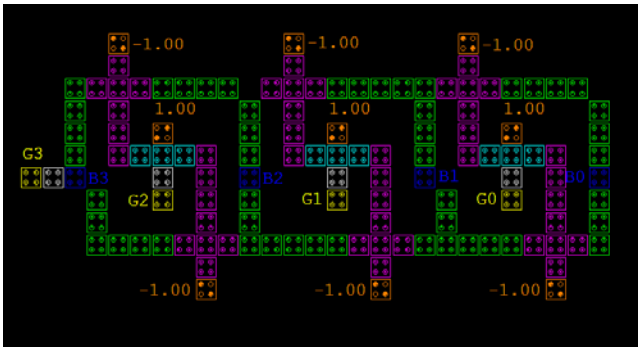


Figure 9. QCA implementation of four bit binary to gray code converter.

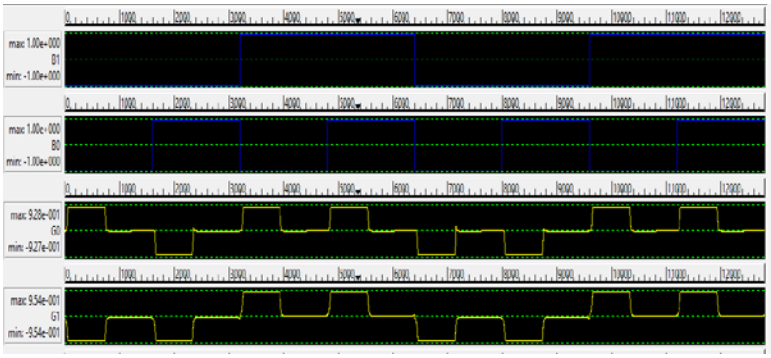


Figure 10. Simulated output of two bit binary to gray code converter.

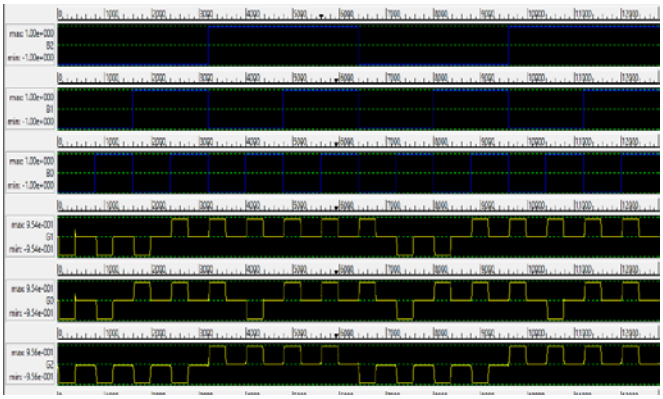


Figure 11. Simulated output of three bit binary to gray code converter

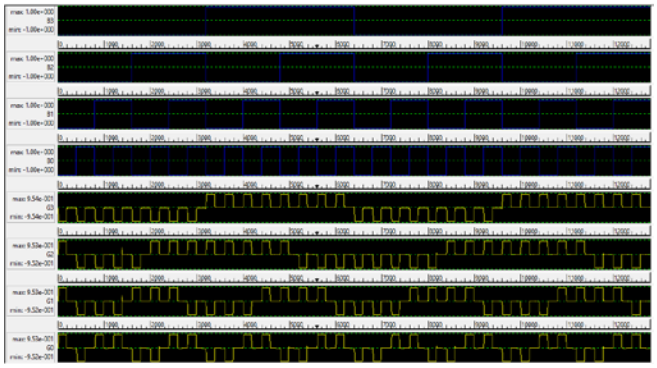


Figure 12. Simulated output of four bit binary to gray code converter.

2.7 Comparative study of proposed design with some recent design layouts–

In this paper we have designed binary to gray code converters up to 4-bits. The novelty of this design besides the parameters like area, usage efficiency, delay and complexity in terms of number of cells is minimal compared to some proposed designs in literature. A comparative study of various parameters of proposed design is performed. Among these our proposed design provides minimal complexity and better efficiency (Table 4 and Chart 1, 2 and 3).

Table -4 Comparison Study of various parameters between previous and proposed design.

		No. of Cells	Area Used(μm^2)	Clock delay
As paper [50]	2-bit	41	0.05	0.75
	3-bit	86	0.12	0.75
	4-bit	131	0.18	0.75
Proposed design	2-bit	38	0.05	0.5
	3-bit	69	0.08	0.5
	4-bit	124	0.13	0.5

Chart 1
Comparative Study of proposed design for the 2-bit binary to gray code Converter

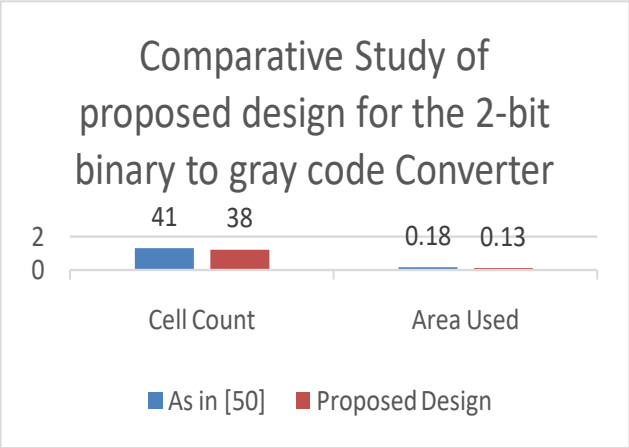


Chart 2
Comparative Study of proposed design for the 3-bit binary to gray code Converter

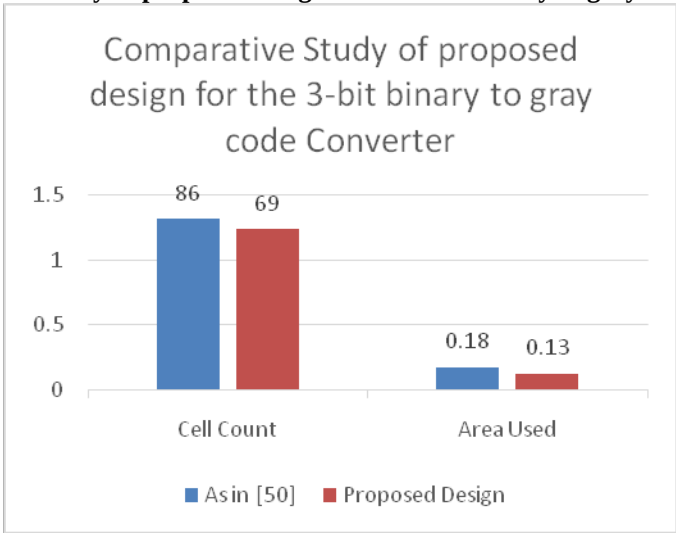
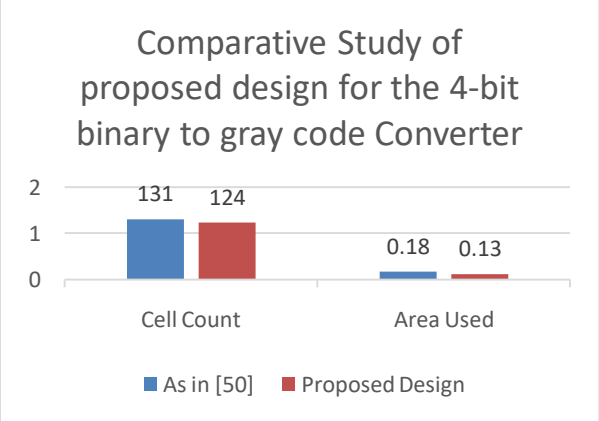


Chart 3
Comparative Study of proposed design for the 4-bit binary to gray code Converter



IV.CONCLUSION

In this paper, a powerful approach for outlining QCA based binary to gray the converter has been introduced in detail. The proposed plans are fit in the way that they encase less number of cells, clock stages, and region. QCA innovation can be the most appropriate option of CMOS based innovation. The simulation results introduce that the proposed circuits execute well. These strategies are favorable in quantum computing, digital signal processing (DSP), and nanotechnology. The proposed outlines could be a promising stride to construct ALU's, show confused circuits in littler measurements and low power design in nanotechnology.

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