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Power Minimization of Full Adder Using Reversible Logic

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ABSTRACT

Adders are normally used for calculating addresses, table indices, and other similar operations in ALUs. They are mostly used in processors. In advanced electronic industry the speed and power of an adder plays a crucial role. Adder almost covers to the total power consumption of the system. Full Adders are frequently required in VLSI and application specific integrated circuits (ASICs). Saving power is one of the biggest concern of the IC industry. Reversible logic is very important in low-power circuit design. Basically reversible circuits do not lose information & reversible computation is performed only when system comprises of reversible gate. In this paper we present the comparison of a reversible full adder and a conventional full adder. Full adder is simulated which is then analysed and comparison has been done on account of the power.

1. INTRODUCTION

Energy dissipation has become one of the dominant issues in present day technology. Energy dissipation occurs due to information loss. This happens in high technology circuits and systems constructed using irreversible hardware. This was demonstrated by R. Landauer in the year 1960[5]. Conventional digital circuits give out a significant amount of energy owing to loss of information. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [4].

A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next

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2. WHY REVERSIBLE LOGIC?

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored

Design constraints for reversible logic circuits [6]:

- Reversible logic gates do not allow fan-outs.
- Reversible logic circuits should have minimum quantum cost.
- The design can be optimized so as to produce minimum number of garbage outputs.
- The reversible logic circuits must use minimum number of constant inputs.
- The reversible logic circuits must use a minimum logic depth or gate levels

3. BASIC REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping [2]. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits

- Number of Reversible gates (N): The number of reversible gates used in circuit.
- Number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate.

The different reversible logic gates are

3.1. Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is $I(A, B)$ and the output vector is $O(P, Q)$. The outputs are defined by $P = A$, $Q = A \oplus B$. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

3.2. Fredkin Gate

Fig 3 shows a 3*3 Fredkin gate. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P = A$, $Q = A'B \oplus AC$ and $R = A'C \oplus AB$. Quantum cost of a Fredkin gate is 5

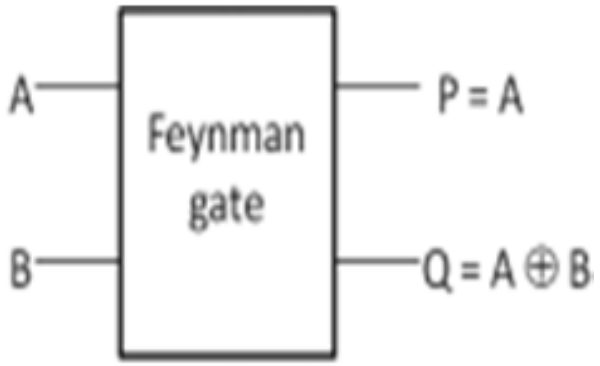

Figure 1: Feyman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 2: Truth Table of Feyman Gate

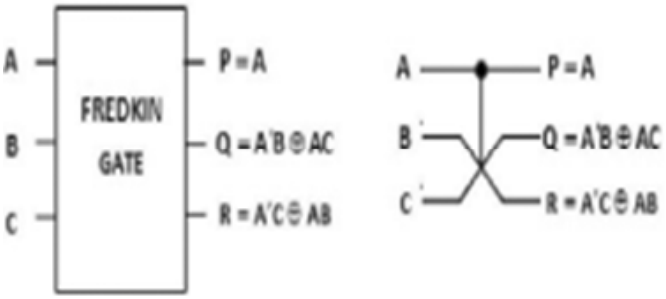

Figure 3: Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 4:Truth Table of Fredkin Gate

3.3. Toffoli Gate

Fig 5 shows a 3*3 Toffoli gate. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The outputs are defined by $P = A$, $Q = B$, $R = AB \oplus C$. Quantum cost of a Toffoli gate is 5.

3.4. Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

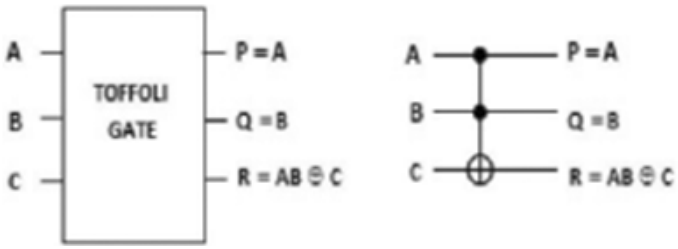

Figure 5: Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Figure 6: Truth table of Toffoli gate

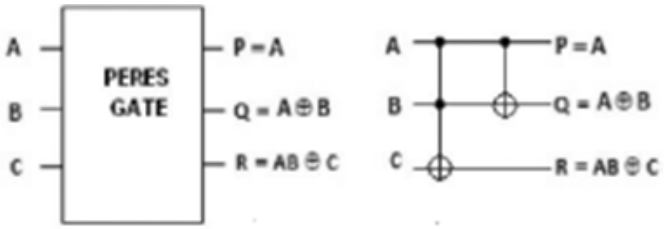

Figure 7: Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Figure 8: Truth Table of Peres Gate

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance. it include the area like

1. Low power CMOS.
2. Quantumcomputer
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair

4. IMPLEMENTATION OF FULL ADDER CIRCUITS

Full adder is the fundamental building block in many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible reversible adder implementations. The full adder circuit's output is given by the following equations:

$$\text{Sum} = A\square \oplus B \oplus Cin$$
$$\text{Cout} = (A \oplus B)\ Cin \oplus AB$$

Synthesis of reversible logic circuits differs significantly from the synthesis of combinational (classical) logic circuits. The reversible logic implementation of full-adder circuit and other adder circuits and their minimization issues has been discussed in [7]. It has been shown in [8] and that any reversible logic realization of full adder circuit includes at least two garbage outputs and one constant input.

In this paper we discuss about the power consumption of a conventional full adder and a revesible full adder

5. SIMULATION RESULTS

The simulation is done using microwind 2.6a. **Microwind** is a tool for designing and simulating circuits at layout level. MICROWIND integrates traditionally separated front-end and back-end chip design into an2 integrated flow, accelerating the design cycle and reduced design complexities. **DSCH** is a software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation.

The simulation results of the conventional full adder and reversible full adder is given in below
The below fig shows the circuit diagram of conventional full adder
The analog simulation of the above circuit is
The below fig shows the circuit diagram of the reversible full adder
The analog simulation of the reversible full adder

6. CONCLUSION

Simulation results shows successful compilations verilog file which is used to make a layout using microwind tool The simulation result given above shows that the power used by the conventional full adder is more than the power used by the reversible full adder.

The simulation results are

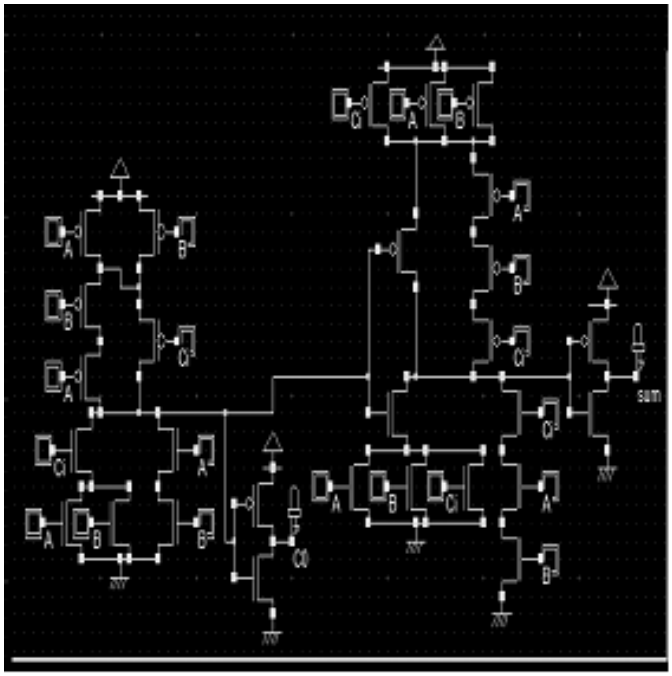

Figure 9: Conventional full adder

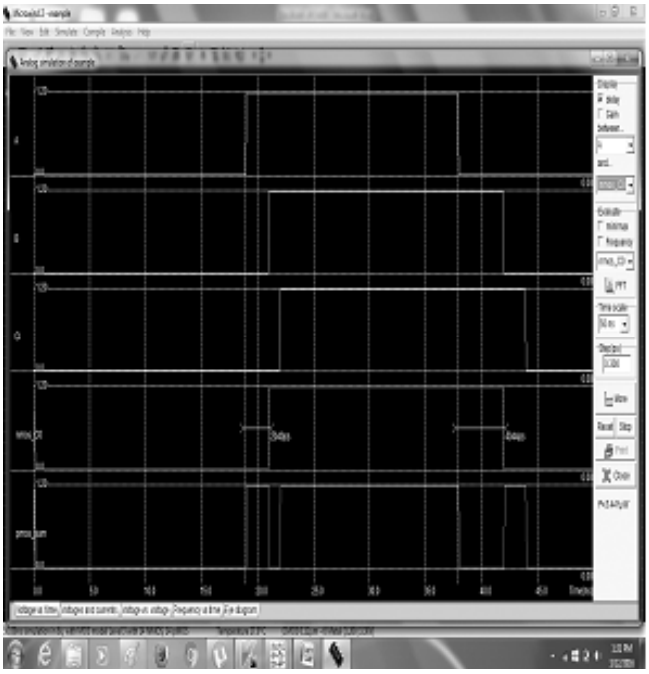

Figure 10: Simulation result of conventional full adder

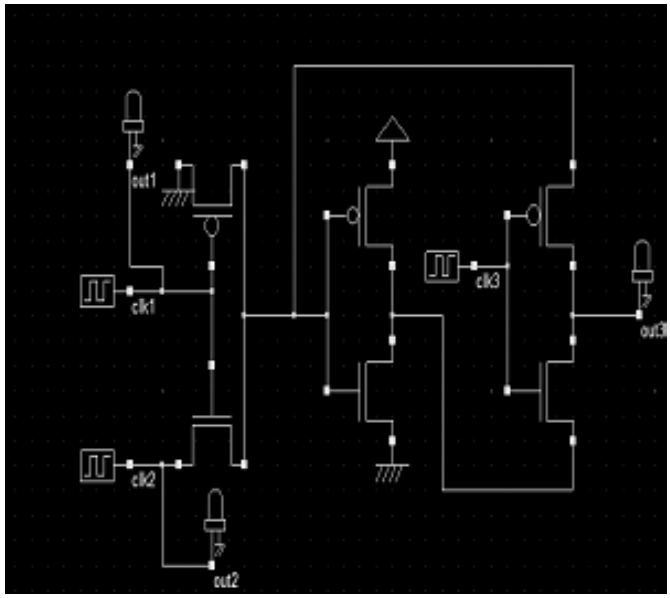

Figure 11: Reversible Full Adder

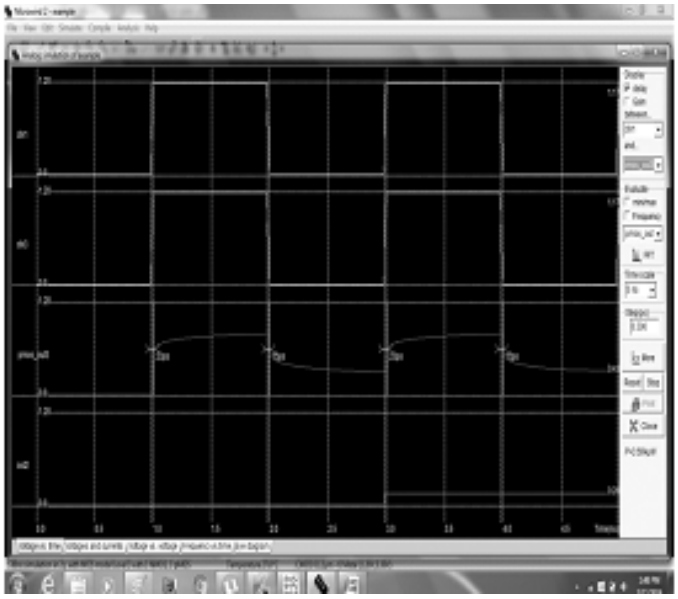

Figure 12: Simulation Result of Reversible Adder

Table 1
Comparison Results

	Power Consumption
Conventional full adder	3.58μw
Reversible Full Adder	3.441μw

REFERENCES

[1] A Novel Quantum Cost Efficient Reversible Full Adder Gate in Nanotechnology By Md. Saiful, Islam Institute of Information Technology, University of Dhaka, Dhaka-1000, Bangladesh E-mail: saiful@iit.du.ac.bd

[2] Introduction to Reversible Logic Gates & its Application B.Y. Prashant. R.Yelekar, Prof. Sujata S. Chiwande *2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications® (IJCA*).

[3] A Review of Reversible Gates and its Application in Logic Design *American Journal of Engineering Research (AJER) e-ISSN: 2320-0847 p-ISSN : 2320*-0936 Volume-03, Issue-04, pp-151-161 www.ajer.org

[4] Bennett C.H., "Logical reversibility of Computation", IBM J. Research and Development, pp. 525-532, 197.

[5] Irreversibilty and Heat Generation in the Computational Process, IBM Journal of Research and Development, R. Landauer, 5, pp. 183-191, 1961.

[6] Raghava Garipelley et al., "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013.

[7] Md. Saiful Islam, Md. Rafiqul Islam, Muhammad Rezaul Karim and Abdullah Al Mahmud, "Synthesis of Adder Circuits using Reversible Logic", In Proc. of 3rd IEEE International Conference for Upcoming Engineers, ICUE 2004, Ryerson University, Toronto, Canada, May 13-14, 2004.

[8] Md. Saiful Islam, Md. Rafiqul Islam, Muhammad Rezaul Karim, Abdullah Al Mahmud and Hafiz Md. Hasan Babu, "Minimization of Adder Circuits and Variable Block Carry Skip Logic using Reversible Gates", In Proc. of 7th International Conference on Computer and Information Technology, ICCIT 2004, Brac University.