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Design and Analysis of Quadrature Voltage Controlled Oscillator for Wireless Communication Standards

Bhavana Bojanapu*, J. Selvakumar and R. Prithivi Raj*****

ABSTRACT

A Quadrature Voltage Controlled Oscillator is proposed which has a locking range of frequencies from 58GHz to 68 GHz. Through symmetrical coupling network formed by diode- connected transistors, the in-phase coupling is realized in IPIC-QVCO, which reduces phase noise and phase error. The entire design is implemented in Agilent ADS (Advanced Design Systems) using 180nm technology. The power consumption of the integrated QVCO is around 16.5mW using a 1.8V power supply. . The objective of this project is to obtain a wide range of higher frequencies which suits for next-generation short range high data rate wireless Communication in the unlicensed 60GHz frequency band. The VCO can tune between 58GHz and 68GHz and exhibits phase noise of -109 dBc/Hz at 100 kHz offset and -136 dBc/Hz at 1 MHz offset respectively.

Index Terms: CMOS, Frequency Synthesizer, In-Phase Injection Coupled (IPIC), Quadrature Voltage Controlled Oscillator (QVCO), Low Phase noise, Low Phase error,PLL.

1. INTRODUCTION

A Quadrature oscillator produces two sine waves with 90° phase difference between them. At resonance, the voltage across a parallel L-C network and the current circulating within it are 90 degrees out of phase. In other words, it means that the circuit has quadrature voltages for two coupled oscillators.

VCOs are used in Function generators, the production of electronic music (generate variable tones in synthesizers), used in Phase-Locked Loops, frequency synthesizers used in communication equipment. Voltage-to-Frequency converters are voltage-controlled oscillators, with a highly linear relation between applied voltage and frequency. Relaxation oscillators are widely used in fully integrated circuits (because they do not have inductors), in applications with relaxed phase-noise requirements, typically as part of a phase-locked loop. However, these oscillators have not been popular in RF design because they have noisy active and passive devices [1]. High-frequency VCOs are usually used in phase-locked loops for radio receivers.

Phase noise is the most important specification for a good oscillator, along with sweep range, linearity, and distortion. . Design of the wide range, low phase noise, low phase error and low power CMOS differential oscillator for higher frequencies is challenging, due to trade-offs between tuning range, phase noise, phase error, and power consumption.

The different methods of generating quadrature LO signals, suffer from many drawbacks as follows [2]. (i) The most common method is through a conventional mm-wave parallel quadrature voltage-controlled oscillator (P-QVCO), but its phase noise is poor [3].(ii) The method of using a divide-by-2 divider after a

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VCO with double LO frequency prevails in multi-GHz applications, but it is difficult to design a VCO and a divider at very high frequency, that consumes higher power.(iii) If passive components such as an RC poly phase filter are used to produce quadrature signals, where it usually need buffers to compensate their loss, which again makes higher power consumption [6].(iv) Using an injection-locked multiplier is a good choice [1], but the disadvantages are limited locking range and intrinsic phase error due to the imbalance of the structure [9].

Comparison of different kinds of VCO:

parameter	Crystal (Tuned Osc.)	LC (Tuned Osc.)	Ring and Relaxation Osc.)
Output frequency	Low	High	Medium
Q Factor	High	Medium	Low
Phase noise	Best	Good	Poor
Power Consumption	Low	High	Highest
Multiphase output	No	No	Yes
Frequency stability	Best	Good	Poor
Tuning range	Narrow	Medium	Wide
Integratability	No	Large size	Small size
Applications	Reference source	GHz VCO	Multiphase VCO, digital clockgeneration

The paper is organized as follows. Section II discusses the Proposed IPIC-QVCO, including architecture, analysis, and circuit design. Section III describes the analysis of oscillation mode. Experimental results are provided in Section IV and conclusions are drawn in Section V.

2. IN-PHASE INJECTION COUPLED QVCO

The proposed QVCO consists of two identical oscillators pulling each other through coupling networks, to lock at a common frequency with quadrature phase [1]. This in-phase coupling can reduce both phase noise and phase error. Injection locking and injection pulling are the frequency effects that can occur when a harmonic oscillator is disturbed by a second oscillator operating at a nearby frequency. When the coupling is strong enough and the frequency is near enough, the second oscillator can capture the first oscillator causing it to have an essentially identical frequency as second; this is injection locking [4].

When the second oscillator merely disturbs the first oscillator but does not capture it, the effect is called injection pulling which is mainly observed in electronic oscillators and laser resonators. In modern day VCO an injection locking signal may override its low-frequency control voltage, resulting in loss of control. When intentionally employed, injection locking provides a means to significantly reduce power consumption and possibly reduce phase noise in comparison to other frequency synthesizers and PLL designs [5].

There are many phase shifting techniques which were presented to realize In-Phase coupling [2].But their coupling networks are either RC based or LC based phase shifters which are both frequency dependent.

The In-phase coupling is realized in the proposed IPIC-QVCO by using the frequency-independent network, instead of the frequency-dependent phase shifter.

The Schematic of the Proposed IPIC-QVCO is shown in Fig.1 [2]. Tuning of L and C gives the required transient response with phase difference varying between 0 to 90 degrees between the signals and yielding L = 45pH and C = 0.11265pF respectively.

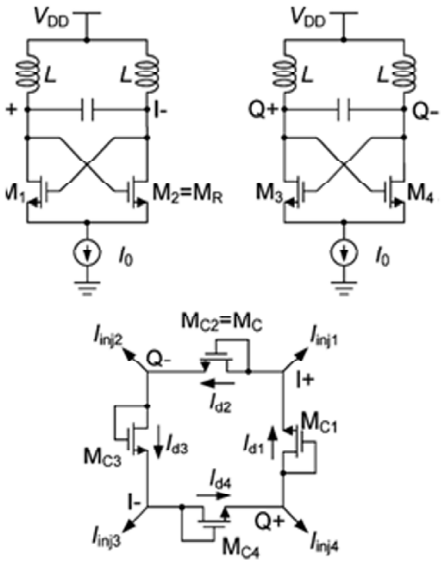

Figure 1: Schematic of the proposed IPIC-QVCO.

2.1. Alternate Model of IPIC-QVCO

An alternate model of the coupling network using VCCS instead of each diode-connected transistor and tank circuits is presented in Fig. 2, which yields the impedance magnitude and phase in Fig.3 respectively.

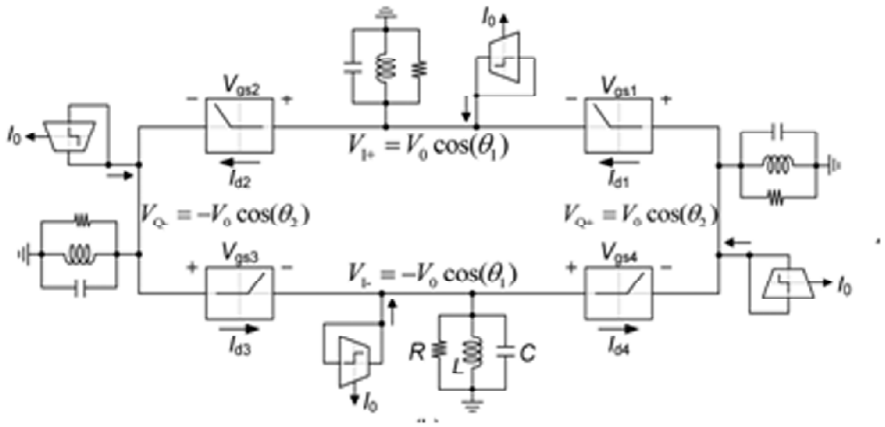

Figure 2: Alternate Model of IPIC-QVCO.

2.2. Magnitude and Phase of LC tank circuit.

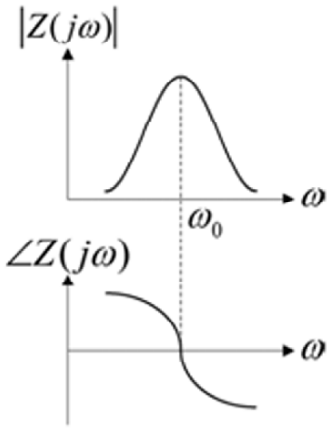

Figure 3: Magnitude and Phase of LC-tank Circuit

3. OPERATION OF IPIC-QVCO,ANALYSIS OF OSCILLATION MODE

The two identical differential *LC* cross-coupled VCOs are coupled through a symmetrical coupling network. In the coupling network, each diode-connected transistor connects.

Two oscillation nodes with π□/2 phase difference [2], like transistor M_{c1} connects node Q+ and node I+ . So the four diode-connected transistors form a symmetrical ring.

Let us assume that the tank Q is high enough that only the fundamental components need to be considered. When the QVCO is operating, M_{c2}'s gate voltage V_g has a phase of 0 degrees, and the source voltage V_s has a phase of -π/2, as shown in Fig. 4(a). Since the amplitudes of V_g and V_s are the same, the gate-source voltage V_{gs} has a phase of π/4. Therefore, the phase of M_{c2}'s drain current I_{d2} is also π/4. M_{c2} is turned on only when V_{gs} is larger than its threshold voltage. The conduction angle is less than, so works in Class-C mode.

Similarly, the phase of Mc2's drain current is 3π/4. The Current I_{inj}, injected into the node I+ from the coupling network, is equal to (I_{d1}-I_{d2}), as shown in Fig. 4(b). Thus, I_{inj} is shifted by exactly π compared with I_{inj} or V_{I+}[2]. A similar situation exists in the other three nodes V_{Q+}, V_{Q+}, and V_{I-}. Therefore, the In-phase coupling is realized in IPIC-QVCO. Since the coupling network does not employ any passive component, it is frequency-independent. As will be demonstrated in simulation and measurement, the parasitic capacitance has little impact on the in-phase coupling even at the mm-wave frequency.

We start with the drain current of a diode-connected transistor in the coupling network. Assuming that its V_s and V_g are $V_0 \cos(\theta_1)$ and $V_0 \cos(\theta_2)$ respectively, where $\theta_1 = \omega t$, $\theta_z = (\omega t + \phi)$, V_0 is the oscillation amplitude, ω is the oscillation frequency and $0 < \phi < 2\pi$. Thus, the gate-source voltage V_{gs} [8] is represented in eq (1)

$$\cos A - \cos B = 2 \sin\frac{B-A}{2} \sin\frac{B+A}{2}$$

$$= V_0\left[2\sin\frac{\theta_1-\theta_2}{2}\sin\frac{\theta_1+\theta_2}{2}\right]$$

If suppose $\theta_2 = B$, $\theta_1 = A$

$$= V_0\left[2\sin\frac{\theta_2-\theta_1}{2}\sin\frac{\theta_1+\theta_2}{2}\right]$$

Since $\theta_1 = \omega t$ and $\theta_2 = \omega t + \psi$

$$= V_0\left[2\sin\frac{\theta_2-\theta_1}{2}\cos\left(\frac{\theta_1+\theta_2}{2}+\frac{\pi}{2}\right)\right]$$

$$= V_0\left[2\sin\frac{\omega t+\psi-\omega t}{2}\cos\left(\frac{\omega t+\psi+\omega t}{2}+\frac{\pi}{2}\right)\right]$$

$$= V_0\left[2\sin\frac{\psi}{2}\cos\left(\omega t+\frac{\psi}{2}+\frac{\pi}{2}\right)\right] \quad (1)$$

The transistor is in the saturation region when it is turned on.

Let $V_s = V_0 \cos\theta_1$ and $V_g = V_0 \cos\theta_2$ where $\theta_1 = \omega t$ and $\theta_2 = \omega t + \varphi$

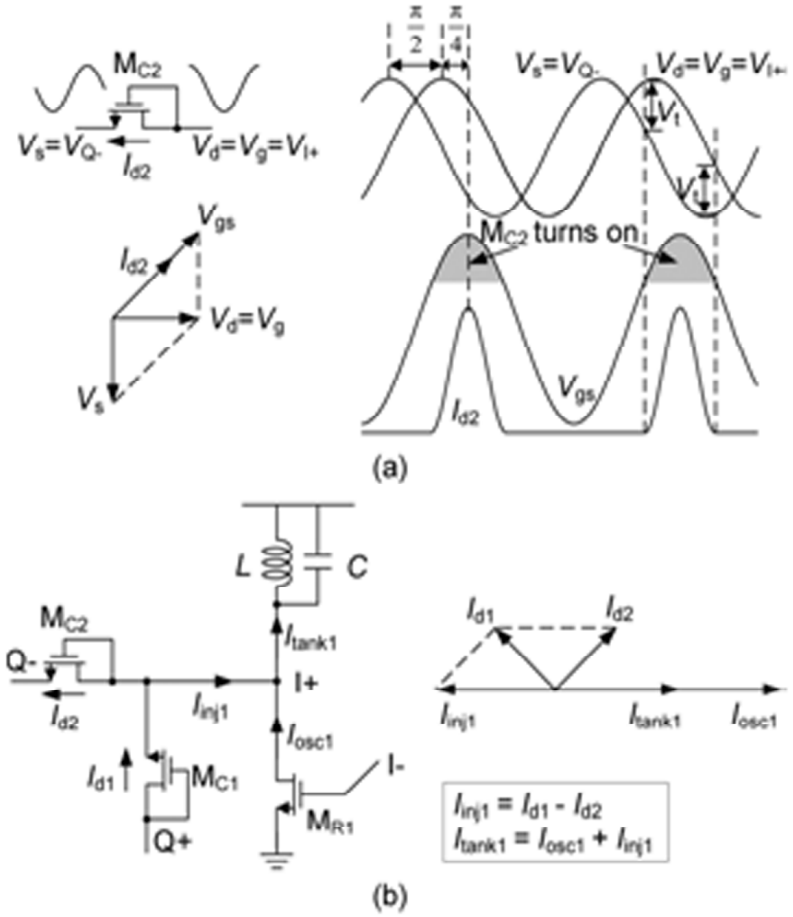

Figure 4: Analysis of (a) diode-connected transistor and (b) coupling network in IPIC-QVCO[2].

Finally

$$V_{gs} = 2\ V_0 \sin\frac{\varphi}{2}\cos\omega t \tag{2}$$

When transistor is on and $V_{gs}>V_t$, then

$$\frac{V_t}{2V_0 \sin\frac{\varphi}{2}} = \cos\omega t$$

$$\omega t = \cos^{-1}\left(\frac{V_t}{2V_0 \sin\frac{\varphi}{2}}\right)$$

Then

$$2\phi = 2\cos^{-1}\left(\frac{V_t}{2V_0 \sin\frac{\varphi}{2}}\right) \tag{3}$$

$$I_d = g_{mK}(V_{gs} - V_t) = g_{mK}\left(2\ V_0 \sin\frac{\varphi}{2}\cos\omega t - V_t\right) \tag{4}$$

3.1. Small Signal Equivalent of negative-Gm Oscillator

The Cross-Coupled NMOS transistors generate a negative resistance, which is in parallel with lossy LC tank.Since the circuit is Symmetric, the controlled sources have the currents as shown below.Equivalent resistance of differential pair

$$Rx = Vx/Ix$$

By Superposition Theorem:

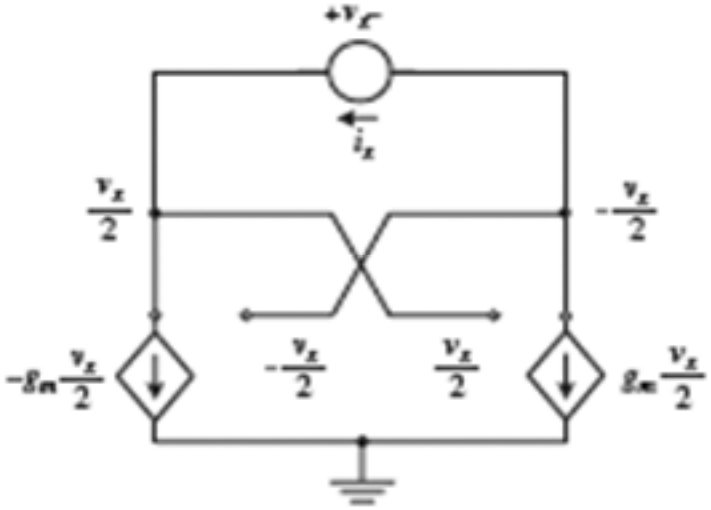

Figure 5: Equivalent Resistance of Differential Pair

$$i_x = -g_m \frac{V_x}{2} + \frac{V_x}{2r_0}$$

$$r_x = \frac{V_x}{i_x} = 2\left(\frac{-1}{g_m} // r_0\right)$$

Since $g_m r_0 >> 1$

$$r_x = \frac{-2}{g_m} \tag{5}$$

Calculation of Gm:

$$g_m = \mu_n C_{ox}\left(\frac{w}{l}\right)\left(V_{gs} - V_{th}\right) \tag{6}$$

Where $\mu_n C_{ox} = 341.4\mu A/V^2$

On substituting Values of L, C as in above equation

(w/l) = 59.99um of M_{c1}.

$V_{gs} = V_g - V_s$

$= 3.3V$

$V_{th} = 0.8V$

We get $g_m = 800156.25*10\text{^}-6$

$= 0.800156.$

Hence, $g_m r_0 >> 1$.

Gain = G_m*(L1//L2)

= G_m*Z_L Where $Z_L = L_1//L_2//C$.

4. SIMULATION RESULTS

An oscillator consisting of two relaxation oscillators that are cross-coupled using two coupling blocks has outputs in very accurate quadrature [8]. The practical results of proposed design are performed in Agilent Advanced Design Systems (ADS) 2015.1.0.The Version using 180 nm Technology respectively.

When two identical oscillators are cross coupled and connected to the symmetrical network ,with respect to Fig. 7.

An Alternate model of QVCO can be designed in the form of bridge rectifier circuit to show how it works in terms of impedance,as shown in Fig. 9.

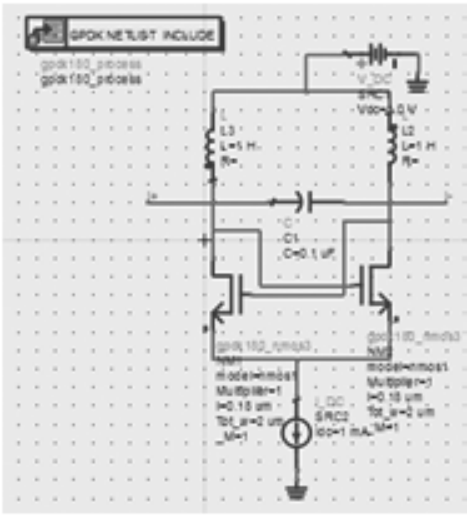

Figure 6: LC-Oscillator Circuit

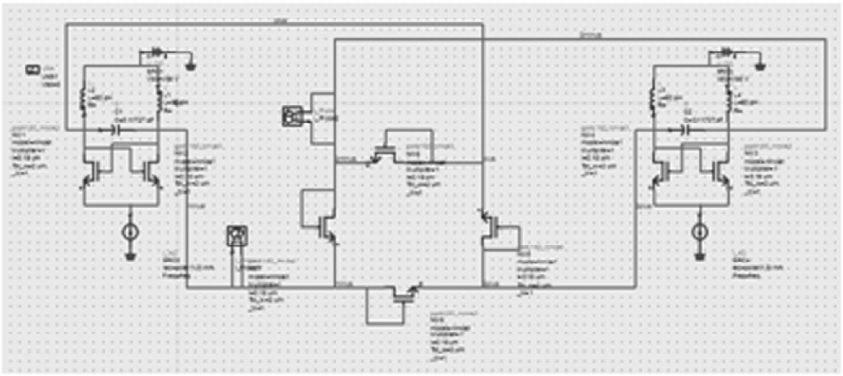

Figure 7: Proposed Quadrature VCO with Symmetrical coupling network.

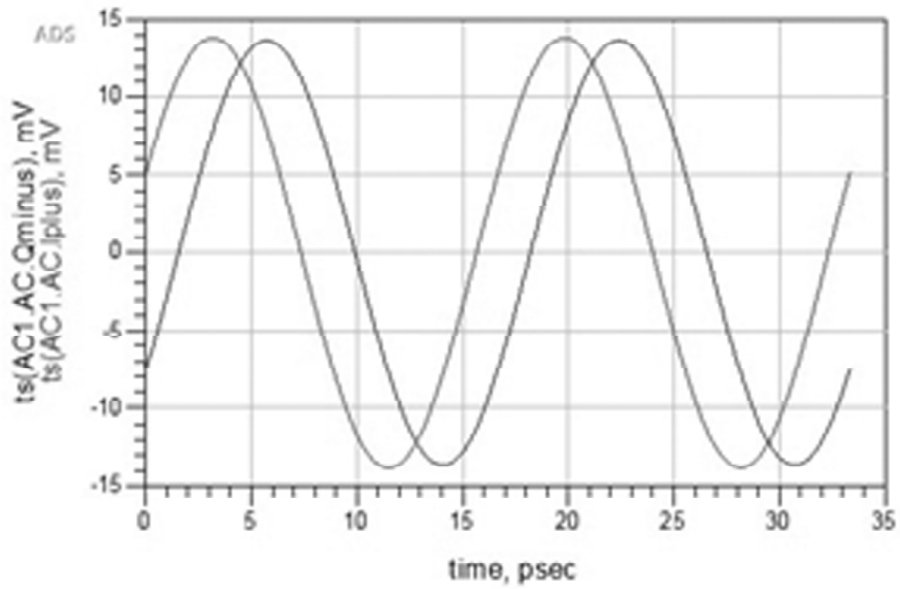

Figure 8: Quadrature phase Analysis of coupling network in IPIC-QVCO.

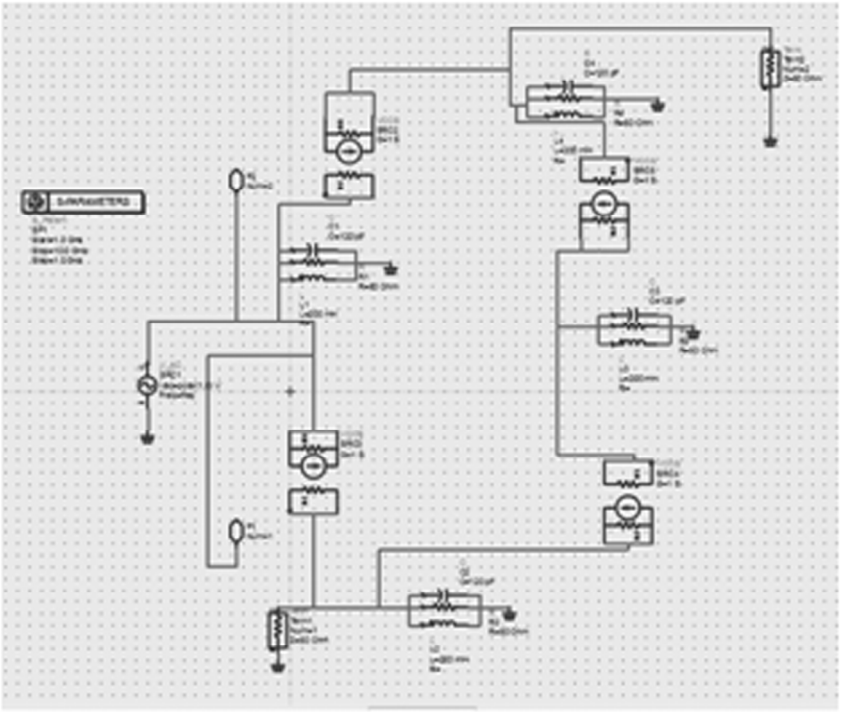

Figure 9: Alternate Model of IPIC-QVCO

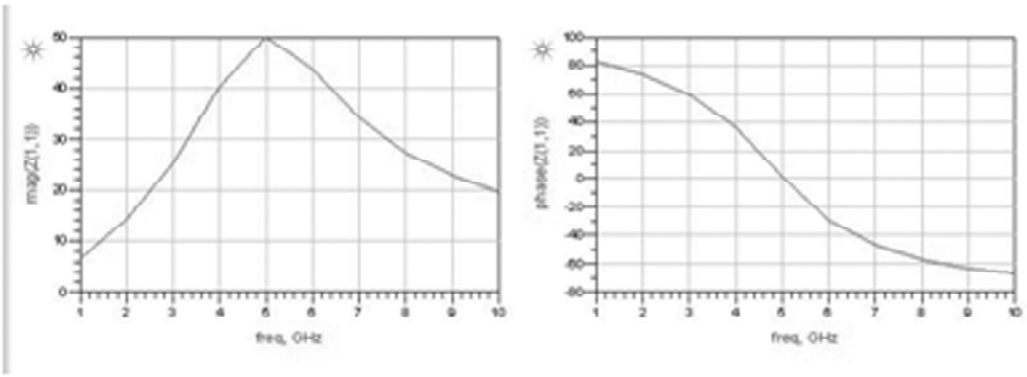

Figure 10: Magnitude and phase of LC tank circuit

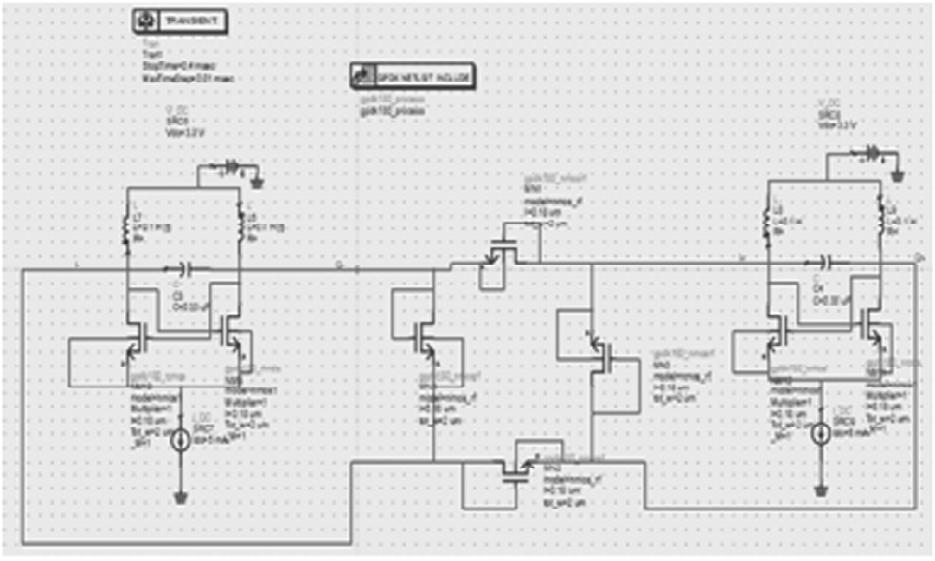

Figure 11: Schematic of IPIC-QVCO in ADS

4.1. Supply Voltage Vs Frequency Response

The design and results have been performed in Agilent advanced design Software. The variation of voltage with respect to frequency is given by Fig .12.

The output waveforms of identical LC-Oscillators along with Symmetrical Coupling network is as shown in Fig.13.

4.2. Transient Response of LC Oscillator

Tuning of L and C parameters in Oscillator circuit gives us the required oscillatory response.

4.3. S- Parameters Analysis:

For a distributed network or RF circuits we talk with the incident and reflected waves in terms of power, and hence, we prefer s –parameters to analyze port matching's or to find reflections at the ports in the circuit.

S-parameter graphs are determined by using simulation-S parameters in ADS. The accurate values of S-Parameters are described below.

The S_{11} also called as input reflection coefficient whose value is around less than 10dB(in fig.15) [7], S_{12} also called as reverse gain ,sometimes called as isolation is always a negative value(in Fig.16),S_{21} called as forward transconductance gain that can be up to -5dB(in Fig.17),S_{22} is called as output reflection co-efficient whose accurate value is less than -10dB(in Fig.18).

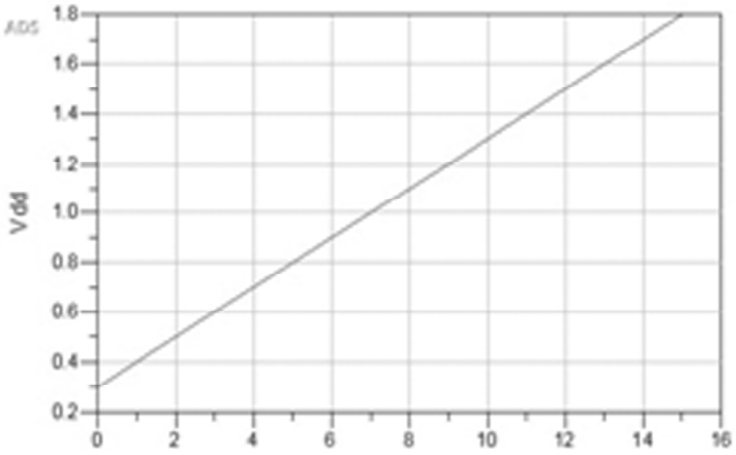

Figure 12: Supply Voltage Vs Frequency

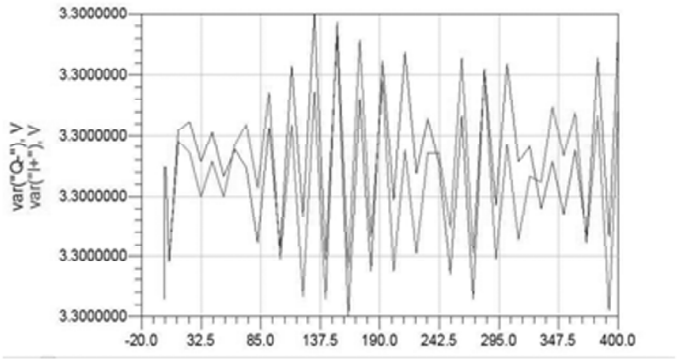

Figure 13: Transient response of IPIC-QVCO circuit

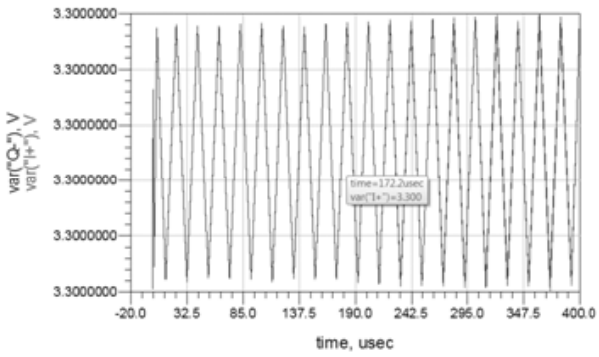

Figure 14: Transient Response of LC-Oscillator after Tuning of LC elements

The S-parameter for the IPIC-QVCO is obtained as shown in Fig. 14, Fig. 15, Fig. 16, Fig. 17 respectively for the proposed QVCO.

With respect to Fig. 15 and Fig. 18 it is clearly seen that S(1,1) and S(2,2) are identical, which means that input and output are perfectly matched. Similarly in Fig.16 and Fig.17 it is observed that the S(1,2) and S(2,1) are also matched since both of them contribute the same graph. From this, it is clearly understood that ports of symmetrical coupling network are perfectly matched.

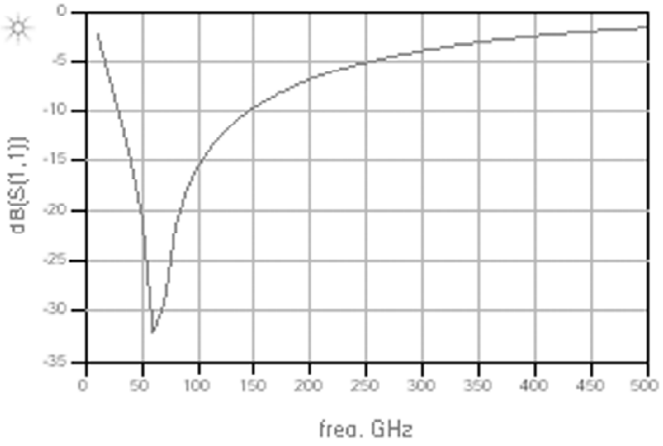

Figure 15: S (1, 1) Input Reflection Coefficient

Figure 16: S (1, 2) Reverse Transconductance Gain

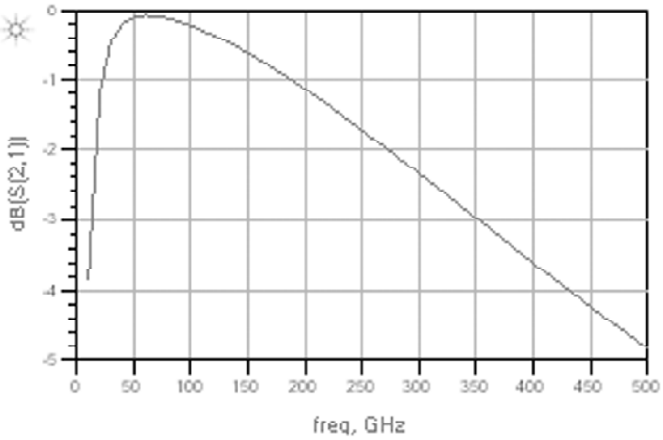

Figure 17: S (2, 1) Forward Transconductance Gain

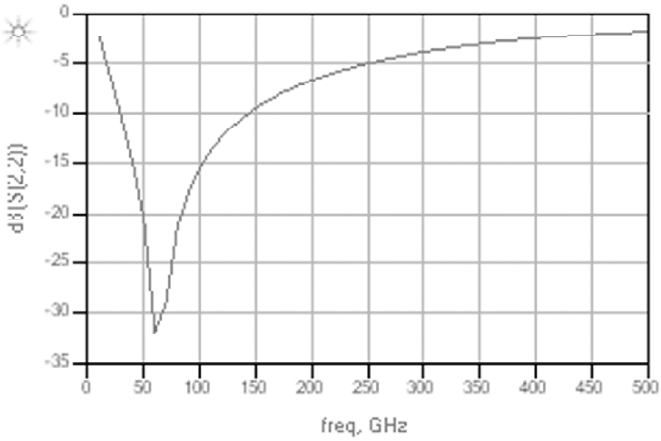

Figure 18: S (2, 2) Output Reflection Coefficient.

4.4. Harmonic balance

Harmonic balance is a frequency-domain analysis technique for simulating nonlinear circuits and systems. It is well-suited for simulating analog RF and microwave circuits since these are most naturally handled in the frequency domain.

4.5. Noise Figure

The noise performance of an RF oscillator is represented by its noise factor or noise figure, which accounts for the degradation of the signal's SNR due to the transmission of a signal from input to output.

$$F = (SNR_{IN}/SNR_{OUT}) \tag{6}$$

where SNR_{IN} and SNR_{OUT} are the SNR's at the input and output of the oscillator respectively. The noise factor represents the signal's quality in terms of noise before and after the network. The noise figure is the same as the noise factor expressed in dB in equation (3).

$$NF(dB) = 10 \log F \tag{7}$$

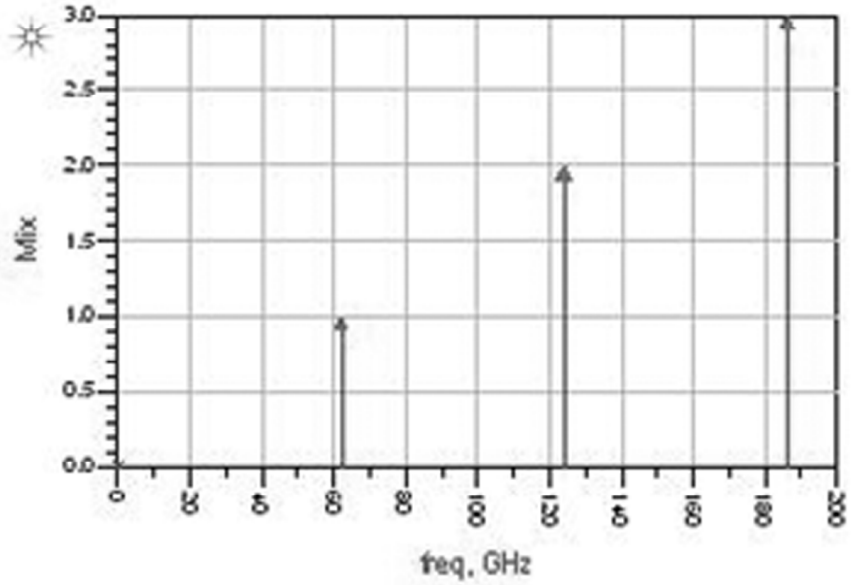

Figure 19: Harmonic Balance of Oscillator

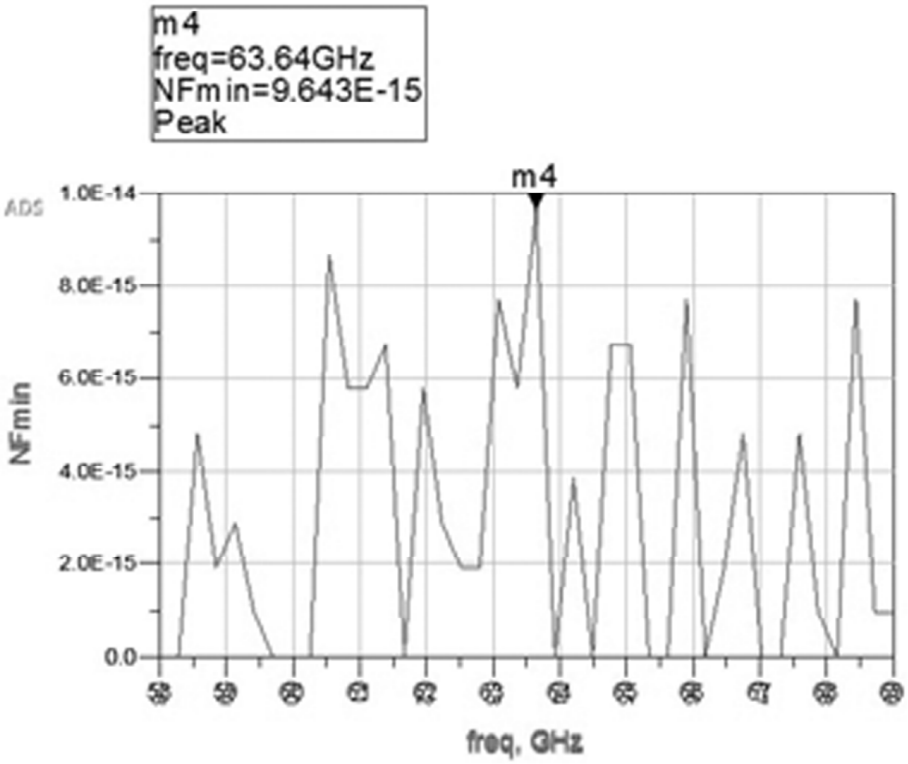

Figure 20: Noise Figure

4.6. Phase Noise

Phase noise is the difference between ideal and practical oscillators.The fluctuations in the output signal due to noise causes signal energies spread across the harmonics of the fundamental frequency,which is known as phase noise.

Phase noise is calculated by using harmonic balance and hb noise controller by taking various parameters into consideration like respective nodes,freq,order,phase noise etc in a display of the corresponding simulators.

Phase Noise Theoritical Calculation:

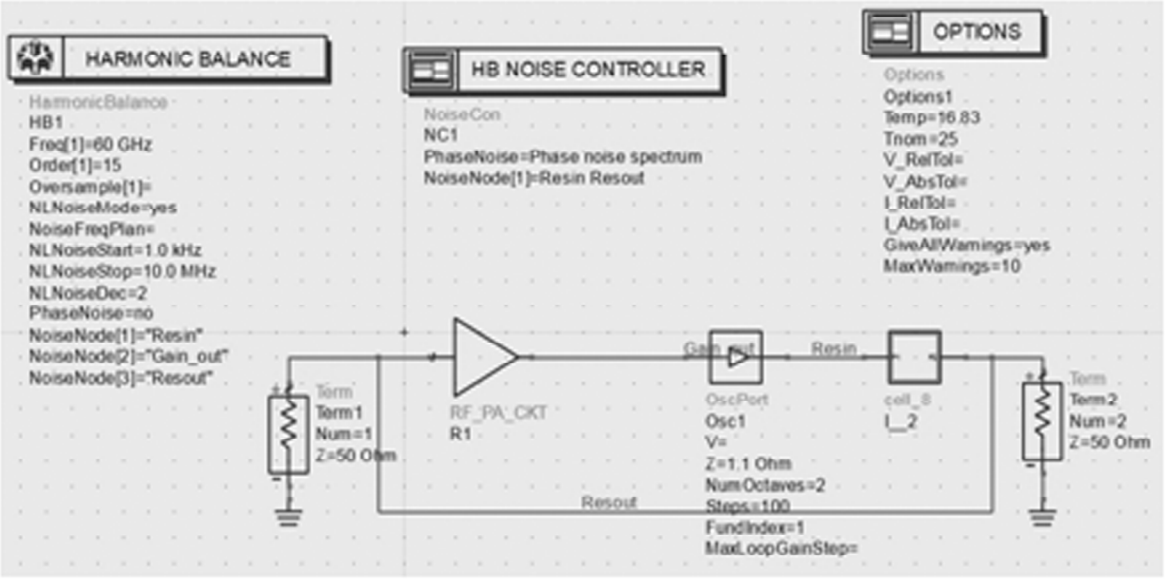

Figure 21: Schematic of finding phase noise in ADS.

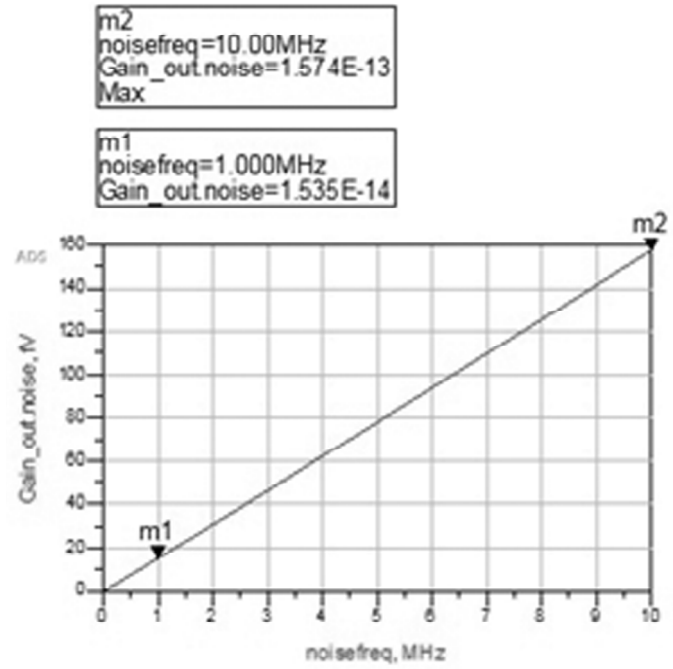

Figure 22: Phase Noise of QVCO in ADS.

$$L(f_m) = 10\log\left[\frac{1}{2}\right]\left[\left(\left(\frac{f_o}{2Q_l f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\right]$$

where f_o = Carrier Frequency (Hz)(100MHz)

Q_l = Loaded Q(72)

f_m = Modulation, baseband, of offset frequency (Hz)(1000)

fc = active device flicker corner (Hz)(1000)

F = amplifier noise factor(5)

k = Boltzmann's Constant

T = Temperature (Kelvin)

Ps = Output power (watts) (23.4mW)

$= 10 \log 4.2946 \times 10^{-14}$

$= -133.67 dBc/Hz$

The measured phasenoise is around -104.5dBc/Hz~-136dBc/Hz respectively at 1MHz offset.

5. CONCLUSION

In this paper, a QVCO with a tuning range from 58GHz to 68 GHz has been proposed which reduces the power consumption required for the circuit since there are no inductor and capacitor in the coupling network. This circuit has been implemented in 180nm CMOS technology and simulated by using ADS. The large frequency span helps to mitigate the impact of variability, which can pose a significant challenge in mm-wave designs. The power consumption of the proposed QVCO is 36.23mW with a phase noise of -109 dBc/Hz at 100 kHz offset and -136 dBc/Hz at 1 MHz offset respectively.

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