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Z Source Multi Level Inverter with Enhanced Performance

B. M. Manjunatha* K. Shaguftha Zabeen and A. Suresh Kumar*****

Abstract : In this paper, a Z Source based balanced capacitor multilevel inverter (ZS-BCMLI) is proposed with a single source and single impedance network. In the proposed ZS-BCMLI, the balancing capacitor circuit is used to balance the voltages across all the capacitors. This circuit not only balances the voltages but also provide a dc link voltage which is 2 times the supplied dc voltage. Hence the fundamental voltage is more than the conventional and recently reported inverters. And also, the magnitude of the fundamental output is not limited to the DC source voltage or the dc link voltage but can be boosted to a wide range by inserting a small shoot through period compared to conventional ZS-MLI's using Impedance Network. The ZS-BCMLI consists of a Z source network to boost and buck the voltage to get a desired output voltage, a balancing capacitor circuit to balance the voltage across all the capacitors fed from a single DC source, a level generator to generate the positive stepped voltage levels across the inverter and one H-bridge for the polarity reversal. The performance of the proposed topology is validated using MATLAB/SIMULINK software.

Keywords : Z Source Inverter, Balanced Capacitor circuit, Multilevel Inverter.

1. INTRODUCTION

Nowadays multilevel inverters are having more and more attention and perfect choice for the applications such as Renewable energy sources, motor drives and FACTS devices because of their high voltage operations and high efficiency [1]. When the number of output levels are more than or equal to three, then the inverters are said to be multilevel inverters. The multilevel inverter synthesizes a dynamic output voltage and produces '*n*' number of levels in the output by using single or multiple DC voltage sources. With an increase in the number of levels, the difference between each voltage step decreases which in turn decreases the total harmonic distortion (THD).

Multilevel inverters are generally classified into three major configurations as Diode-clamped, flying capacitor and cascaded H-bridge multilevel inverters [2-4]. The major advantage of these multilevel inverters is their step-wise output voltage which results in high power quality, better electromagnetic compatibility, higher voltage capability and may lead to elimination of the coupling transformers at distribution voltage level, there by decreases the cost. Also, in these multilevel structures, higher output voltage with lower harmonics can be achieved with enhancement the number of voltage levels without increasing the rated power of each device.

Despite the advantages of the above mentioned conventional MLI's, the number of power switches, gate driving circuit's, heat sinks and protection circuits increases with an increase in the number of levels

* Associate Professor, Dept of EEE, RGMCET, Nandyal, India 518501. manjunath.bmeee@gmail.com

** PG scholar, Power Electronics, RGMCET, Nandyal India, 518501. shaguftha27@gmail.com,

*** Associate Professor, Dept of EEE, RGMCET, Nandyal, India 518501. surianisetty@gmail.com,

that makes the inverter more complex and bulky. In diode clamped MLI, (*n*-1) capacitors are used as a potential divider. This series connected dc-link capacitors of a diode-clamped multilevel inverter suffers from a voltage imbalance issue because of unequal capacitor charging and dis-charging and it also requires (*n*-1) * (*n*-2) clamping diodes. In flying capacitor MLI, (*n*-1) * (*n*-2) /2 flying capacitors are required. When inverter operates at lower frequencies the size and cost of the inverter increases. In cascaded H-bridge type multilevel inverter, independent dc-link voltage need to be provided for each cell.

To reduce the number of power switches many topologies has been proposed with less number of switches [5-9], whereas these inverters require more than one DC source which leads to imbalance in the voltages when they are supplied from a renewable energy sources. Many voltage balancing techniques have been proposed to solve this dc –link capacitor imbalance problem. The easiest approach is to supply the capacitors with separate reversible sources [10]. Utilizing back-to-back inverters is another option [11-12]. In [13], the rectifier-inverter stages are controlled in order to achieve capacitor voltage balance. In [11, 12], the rectifier and the inverter are separately controlled and in [12, 14] redundant switching states are used to control the capacitor voltages. Alternatively, auxiliary circuits can be added to achieve capacitor voltage balance: three-level [15, 16], four-level [17, 18] and five-level [19, 20]. These circuits transfer energy from the higher capacitor voltage to an adjacent lower capacitor voltage and these additional circuits for balancing lead to increase in the control complexity, size and cost of the inverter.

In all the above mentioned ML's, each level of output voltage cannot increase beyond the dc source voltage and for boost or buck the dc voltage, other converters such as d-dc converter must be used. This type of inverters requires additional components for boosting the voltage and it is two stage converters. The output voltage can be boosted in a single stage by employing the Z-source network instead of dc-dc converters [21]. Z-source MLI is a kind of single stage multilevel inverter which has the ability of voltage boost. It employs an impedance circuit which connects the power source to the inverter circuit thus providing a unique feature which cannot be obtained in the conventional Voltage Source Inverter (VSI) uses a capacitor and Current Source Inverter (CSI) uses inductor. The Z-source inverter overcomes the limitations of the traditional VSI and CSI. Inverter (VSI) can only produce an output voltage which is equal to the supply voltage. The maximum output voltage obtainable is limited by the DC bus voltage. Hence Z-source inverter has the useful feature to either buck or boost the batteries voltage to a desired output voltage through shoot through state and non-shoot through state control. Several pulse width modulating and boosting techniques are proposed in the literature for Z source inverter (ZSI) [22] for two and multi levels.

This paper presents novel MLI topology that is capable of maintaining the equal voltage across all the flying capacitors, which is capable to provide the more fundamental voltage without inserting the shoot-through also and which is capable to boosts the output voltage to required level by controlling the shoot-through period. It consists of single DC source, single impedance network with DC link capacitors, flying capacitors, clamping switches, level generator and single H-bridge. The performance of the proposed topology is validated using MATLAB/SIMULINK software.

The rest of the paper is organized as follows: Operating modes of ZSI are discussed in section 2, the new MLI with capacitor voltage balancing is explained in section 3, single Z-source based MLI is discussed in section 4, simulation results are presented in section 5 and finally conclusions are made at the last of all sections.

2. Z SOURCE NETWORK

Z source inverter (ZSI) consists of a two-port impedance network that connects the inverter main circuit to the dc source voltage, load or another converter. The dc source may be a voltage source or a current source. Therefore the dc source can be a battery, diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor or a combination of those. The two port impedance network consists of two symmetrical inductors L1 & L2 and to symmetrical capacitors C1 & C2 connected in X-shape. Fig.1

shows the representative diagram of a 1–∅/3–∅ two-level or multilevel inverter. Diode D is employed between the input dc source and impedance network to resist the reversal flow of current. The concept of the Z source can be effectively applied to all dc-dc, dc-ac, ac-ac and ac-dc power conversions.

A diode D and impedance network are the only difference between a traditional voltage source two-level or multilevel inverters. The conventional inverter will operates only in two states i.e., active state and null state. Whereas, this ZSI operates in one extra state called shoot-through state along with the active and the null states. The performance of ZSI during six active states and in the null state is same to that of the conventional VSI/CSI's. ZSI performs the boost operation by effectively utilizing the shoot-through state. This shoot-through state is not used, when the d input voltage is enough to produce the required ac voltage with good performance. Hence during this, the ZSI acts as a buck inverter just like a VSI.

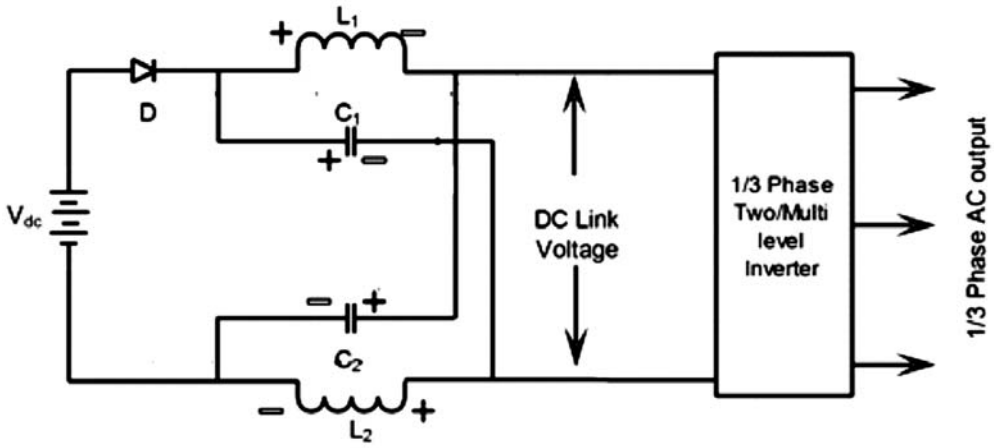


Fig. 1. Z source inverter.

Mode 1: Null State

The Null state can also be called as Zero state. In this state, the ZSI performs as the conventional inverter. The null state can be obtained in two ways *i.e.*, by turning ON all the upper switches at the same instant or by turning ON all the lower switches at the same instant. By doing so, the inverter is disconnected from the source and the output voltage of an inverter during this state is zero as the load terminals are short circuited. The equivalent circuit of the Z source inverter during the Null state operating mode is shown in fig.2.

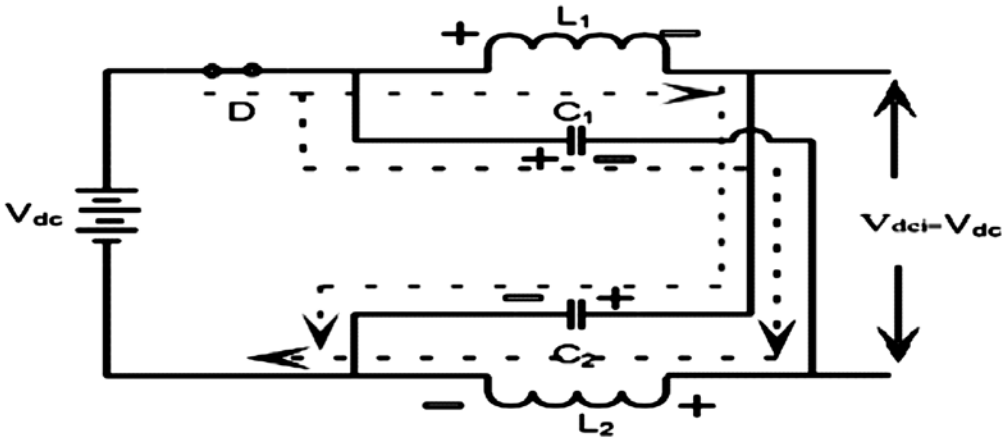


Fig. 2. Equivalent circuit of ZSI in null state.

Where:

V_{dc} : supply voltage;

V_{dci} : voltage across the Z network or input to the inverter main circuit.

During this state, the diode D at the input side of an impedance network becomes forward biased and since the inverter is disconnected from the supply, the capacitors C_1 and C_2 charges to the supplied voltage V_{dc} through the current paths shown in the above figure. The input voltage to the inverter V_{dci} is equal to V_{dc} and the output voltage of an inverter becomes 0.

Mode 2: Shoot-through State

This state is unique for the ZSI and cannot be applied for traditional VSI. The shoot through state can be obtained by turning on the switches of inverter leg at same instant or it can also be inserted by connecting a switch S_{sh} across the impedance network and by turning on the switch at a regular intervals. Hence, during this state the inverter is represented by a short circuit as shown in fig.3. The sum of the voltages across the Z source capacitors C_1 and is greater than the supply voltage which makes the diode (D) reverse biased. Therefore, the supply voltage is completely isolated from the inverter.

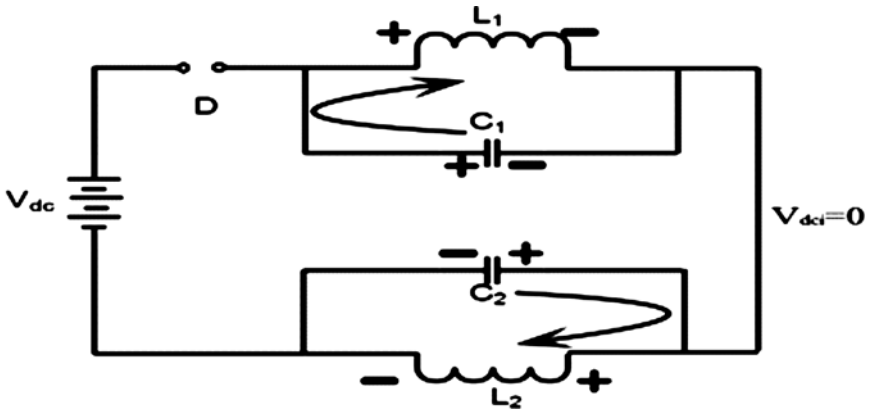


Fig. 3. Equivalent circuit of ZSI during shoot-through state.

The voltage equations during this mode are given in (1).

$$V_L = VC;\ V_d = 2V_{dc};\ V_{dci} = 0 \quad (1)$$

Where, V_d is the voltage at the diode, V_L and V_C is the voltage across the inductor and capacitor respectively.

Mode 3: ACTIVE STATE

In this state, the inverter operates in any one of the six active states and it acts as a normal conventional voltage source or a current source inverter. During this state, any excessive energy stored in the impedance network is discharged to the supply to maintain stability of the capacitors and inverter voltages. Thus, dc link voltage is boosted to the amount of shoot through period is inserted during the shoot through state. The equivalent circuit of the Z source inverter during the Active period is represented in fig.4.

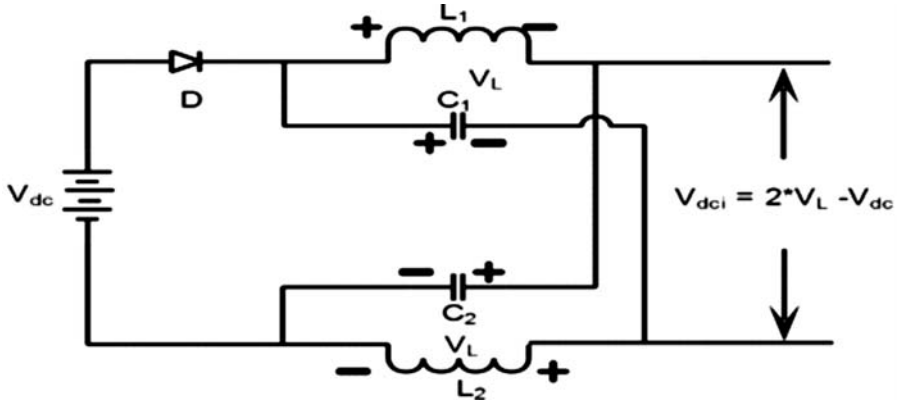


Fig. 4. Equivalent circuit of ZSI in active state.

The voltage equations during this mode are given in Eqn.(2).

$$V_L = V_{dc} - V_C \quad V_{dci} = V_C - V_L = 2V_C - V_{dc} \tag{2}$$

The boost factor is given by Eqn. 3 as,

$$B = \frac{1}{1 - \frac{2 \times T_{sh}}{T}} \tag{3}$$

Where, T_{sh} is the shoot through period and T is the total time period.

3. NEW MLI WITH SINGLE SOURCE

A multilevel inverter with reduced number of switches compared to conventional MLI's, fed from a single dc source for n levels is shown in fig.5. It consists of two parts, part1 and part 2. Part 1 is composed of level generator with $\frac{(n-1)}{2}$ switches that are used to generate the required positive voltage levels across the inverter and part 2 is composed of a single H-bridge cell with four switches that are used for the polarity reversal to get the ac voltage at the output side of an inverter.

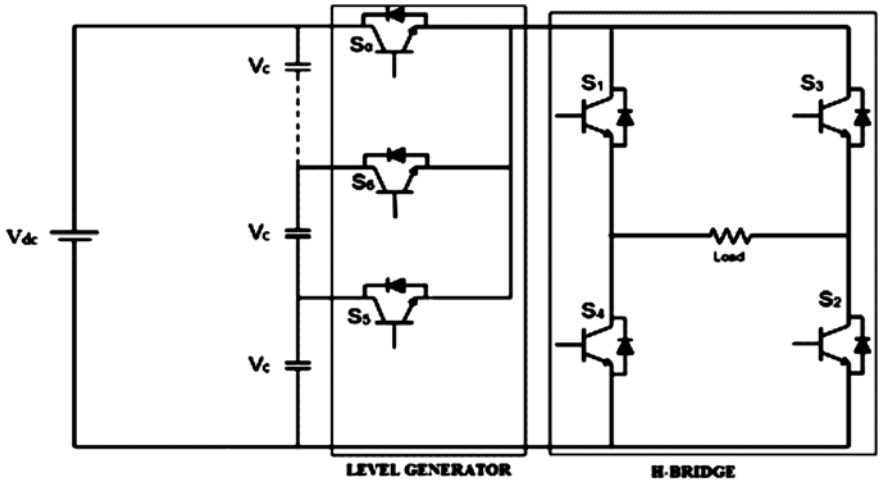


Fig. 5. New MLI with single source and reduced number of switches.

Thus the multilevel structure which is shown in fig. 5 uses a total of (n + 7)/2 switches including (n–1)/2 switches of the level generator and 4 switches of H-Bridge to generate the 'n' number of levels on the output phase voltage with one DC source. This structure uses less number of components compared to the conventional multilevel inverters. Hence, the controlling of the circuit becomes very simple and also the size and cost of the circuit reduces. The similar structure is explained in [23] it requires (n-1)/2 sources. The number of capacitors required and peak output voltage is given in equation (4) and (5).

Number of capacitors required,

$$N_C = \frac{n-1}{2} \tag{4}$$

The peak output voltage, $$V_p = \pm n \times V_c \tag{5}$$

Where, n is the number of output levels to be generated and V_c is the voltage across each capacitor.

The above mentioned topology which is shown in Fig.5 is augmented for five levels with 6 switches ($S_1 - S_6$), 2 flying capacitors (C_1 & C_2) and one dc source is represented in the Fig.6. The Positive voltage ($+ V_c$) at the output side of an inverter is obtained by turning on the switches S_1, S_2 & S_5 .Similarly, the negative output voltage ($-V_c$) is obtained by turning on the switches S_3, S_4 & S_5. The switching sequence to generate the voltages up to n levels at the output side of an inverter is represented in Table.1.

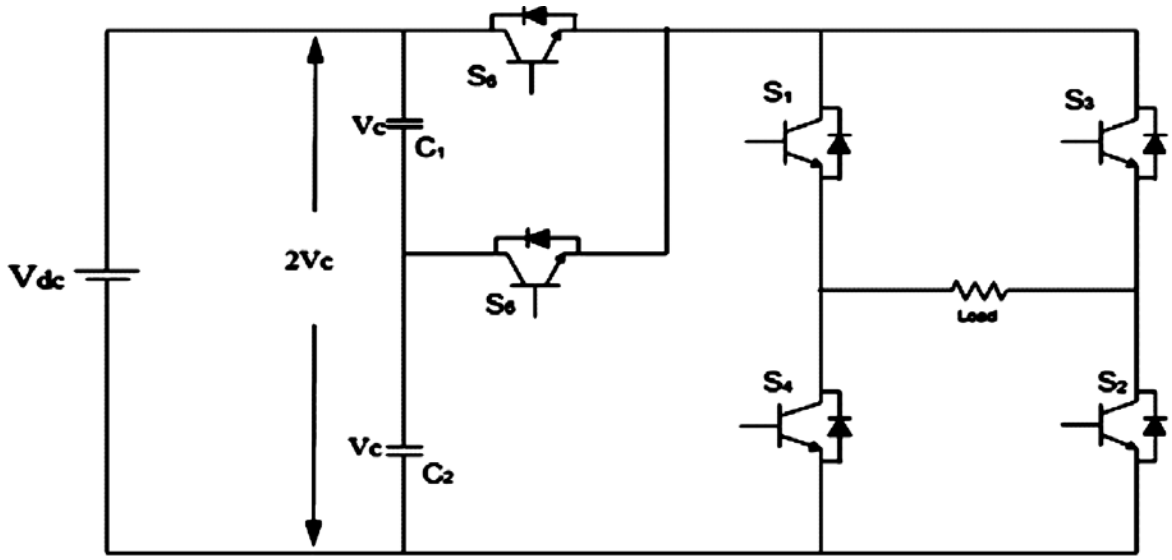


Fig. 6. Five-level Inverter with single source.

Table 1. Switching sequence for new MLI with single source.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	…	S_∞	V_o
H-Bridges switches					*Levels generating switches*				
1	0	1	0	0	0	0	…	0	0
0	1	0	1						
1	1	0	0	0	0	0	…	1	$+ n \times V_c$
.	.	.	.	.	.	.	…	.	.
.	.	.	.	.	.	.	…	.	.
1	1	0	0	0	0	1	…	0	$+ 3 \times V_c$
1	1	0	0	0	1	0	…	0	$+ 2 \times V_c$
1	1	0	0	1	0	0	…	0	$+ 1 \times V_c$
0	0	1	1	1	0	0	…	0	$- 1 \times V_c$
0	0	1	1	0	1	0	…	0	$- 2 \times V_c$
0	0	1	1	0	0	1	…	0	$- 3 \times V_c$
.	.	.	.	.	.	.	…	.	.
.	.	.	.	.	.	.	…	.	.
0	0	1	1	0	0	0	…	1	$- n \times V_c$

In the fig.6 it is assumed that the applied voltage V_{dc} is equally distributed across the two flying capacitors C_1 and C_2, but in practical it is not equal. For the applied input voltage V_{dc}, the voltage distribution across the two flying capacitors is shown in Fig.7. From fig.7, it can be seen that the voltage distributed across the capacitors is different, hence it results in a large step change in the output voltage, which tends to increase the output THD as shown in fig.8.

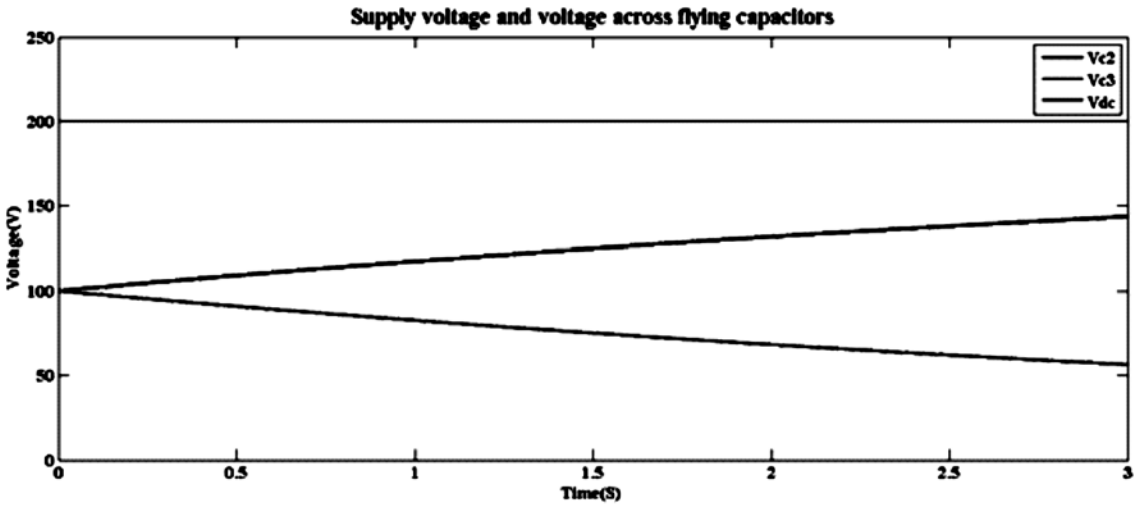


Fig. 7. Input voltage and Unequal voltage distribution across flying capacitors.

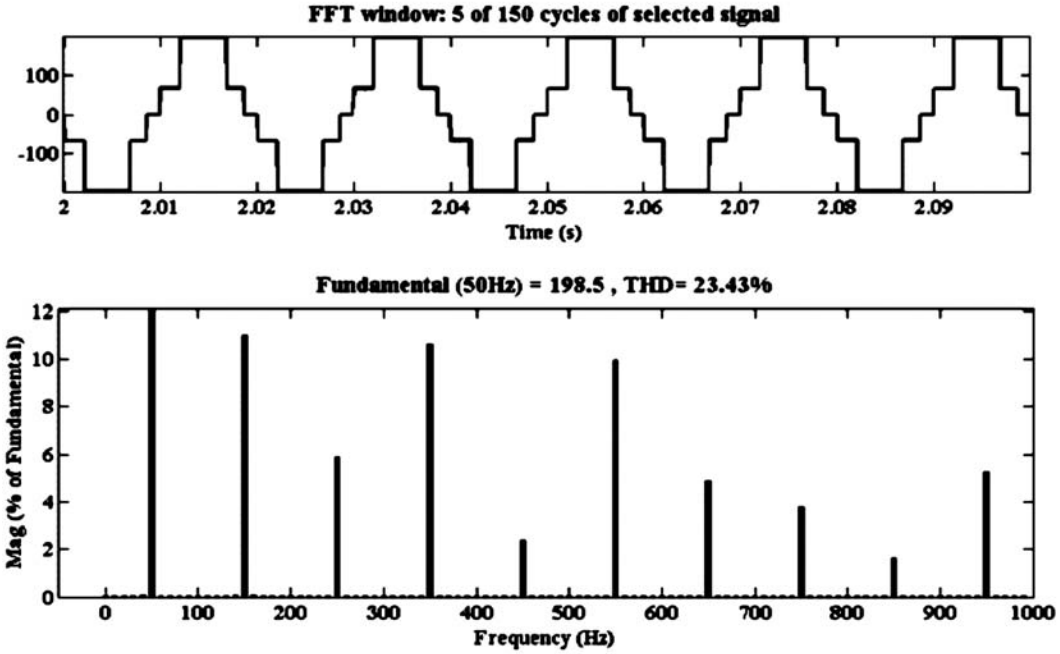


Fig. 8. (*a*) Output voltage and (*b*) THD spectrum of new five-level inverter without capacitor balancing circuit.

To overcome the voltage unbalance problem which is the predominant issue in the previous circuit of fig.6, a new circuit with balanced capacitor is added to it and is shown in fig.9.

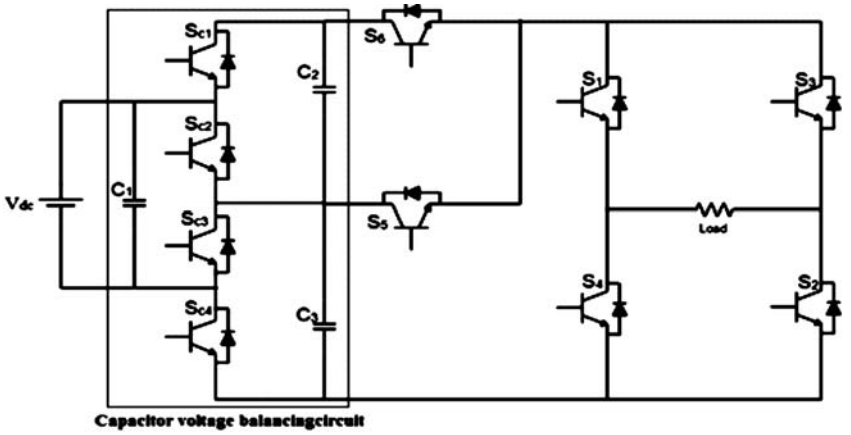


Fig. 9. New Five-level Inverter with capacitor voltage balancing circuit.

Fig.9 shows the structure of five-level inverter with capacitor balancing circuit. This new five-level inverter is composed of balancing capacitor part along with the level generator and H-bridge. Balanced capacitor part consists of clamping switching devices Sc_1 to Sc_4 operated at higher frequency and three capacitors C_1 to C_3 out of which C_1 is the DC link capacitor, C_2 and C_3 are flying capacitors. A level generator consists of two switches S_5 and S_6 and the polarity reversal unit (H-Bridge) consists of four switches S_1 to S_4. The switches S_1 to S_6 operates at the fundamental frequency and clamping switches operate at higher frequency.

$$\text{Number of dc link capacitors required} = \frac{(n-3)}{2} \tag{6}$$

$$\text{Number of flying capacitors required} = \frac{(n-1)}{2} \tag{7}$$

$$\text{Number of clamping switches required} = (n-1) \tag{8}$$

Capacitor Balancing Part

If the multilevel inverter which is shown in fig.9 operates without the capacitor balancing circuit, then the voltages across the flying capacitors would be unbalanced due to the asymmetrical charging and discharging of the current through the capacitors, which also happens in the conventional topologies when they are fed from a single DC source. Hence, here the capacitor voltage balancing part plays a vital role in balancing the voltages of capacitors by alternative conduction of the clamping switches $S_{c1} - S_{c4}$.

The balanced capacitor part operates with two kind of working states. The clamping switches $S_{c1} - S_{c4}$ are divided into two groups as group 1 and group 2. Group 1 is composed of switches S_{c1} and S_{c3} and Group 2 is composed of S_{c2} and S_{c4} *i.e.*, all the even switches belong to the same group and all the odd switches belong to one group which is other than the group of even switches. The switching of these two groups is complimentary to each other *i.e.*, when the switches of group1 are conducting, then the switches of group 2 must be turned off and vice versa.

When the switching devices of group 1 are ON and group 2 are OFF, then the switches of group 2 becomes open circuited and thus C_1 becomes in parallel with the flying capacitor C_2, hence $V_{c1} = V_{c2}$ and if the source is connected across the dc link capacitor C_1, then the voltage across the capacitors C_1 and C_2 becomes equal to the supplied voltage (*i.e.*, $V_{c1} = V_{c2} = V_{dc}$). The equivalent circuit of the inverter in fig.9 during group1 switching state is shown in fig.10.

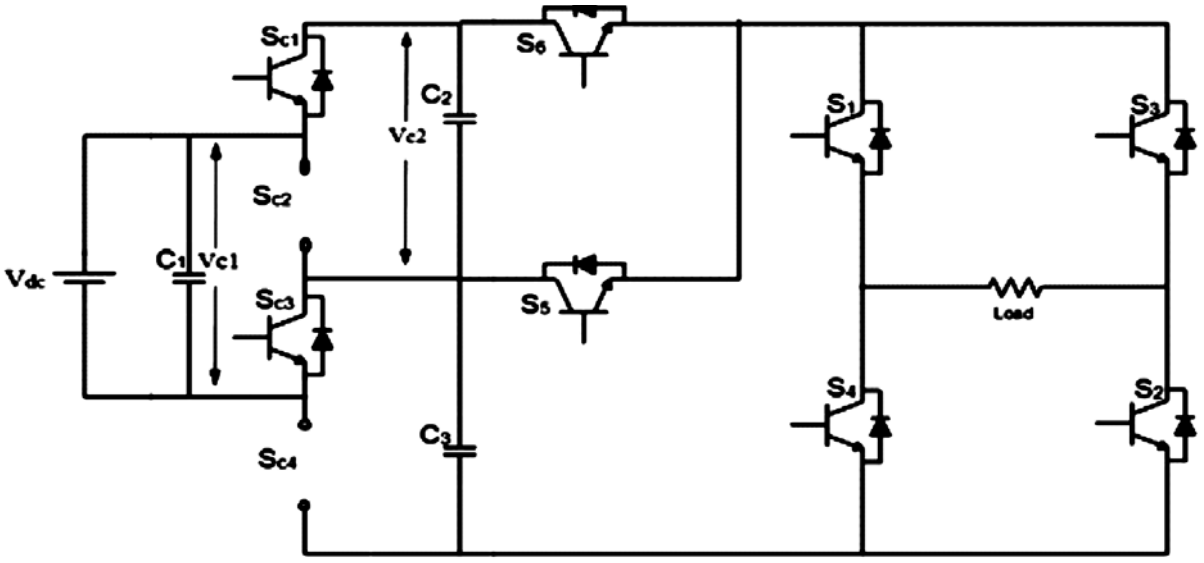


Fig. 10. Equivalent circuit of five-level Inverter when group 1 switches of Capacitor-balancing part are conducting.

When the switching devices of group 2 are ON and group 1 are OFF, then the switches of group 1 becomes open circuited and thus C_1 becomes in parallel with the flying capacitor C_3, hence $V_{c1} = V_{c3}$ and if the source is connected across the dc link capacitor C_1, then the voltage across the capacitors C_1 and C_3 becomes equal to the supplied voltage (*i.e.*, $V_{c1} = V_{c3} = V_{dc}$). The equivalent circuit of the inverter shown in fig.9 during group2 switching state is shown in fig.11.

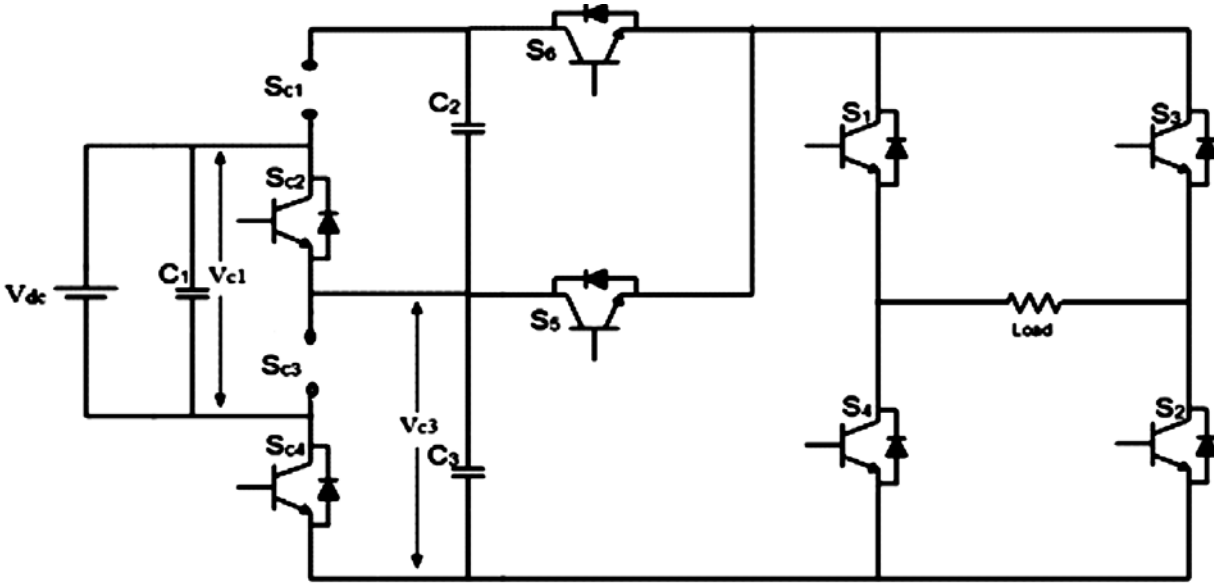


Fig. 11. Equivalent circuit of five-level Inverter when group 2 switches of Capacitor-balancing part are conducting.

Hence, from the two equivalent circuits of the five-level inverter with single source when capacitor balancing part is adopted, it can be seen that the voltages of the capacitors can be keep in balanced by switching group1 or group2 once in every periodic cycle. Thus, the voltage across the flying capacitors is maintained balanced and the dc link voltage will becomes twice the input voltage because in group1 switching state, the entire applied voltage is appeared across the capacitor C_2 and in group 2 switching state, the applied voltage is appeared across the flying capacitor C_3, then $V_{c2} = V_{dc}$, $V_{c3} = V_{dc}$, therefore, $V_{c2} + V_{c3} = 2V_{dc}$ and thus output voltage is doubled. The capacitor balancing circuit not only balances the voltage across all the capacitors but also increases the fundamental voltage for the applied voltage V_{dc} as shown in fig.12, fig.13 and fig.14 respectively.

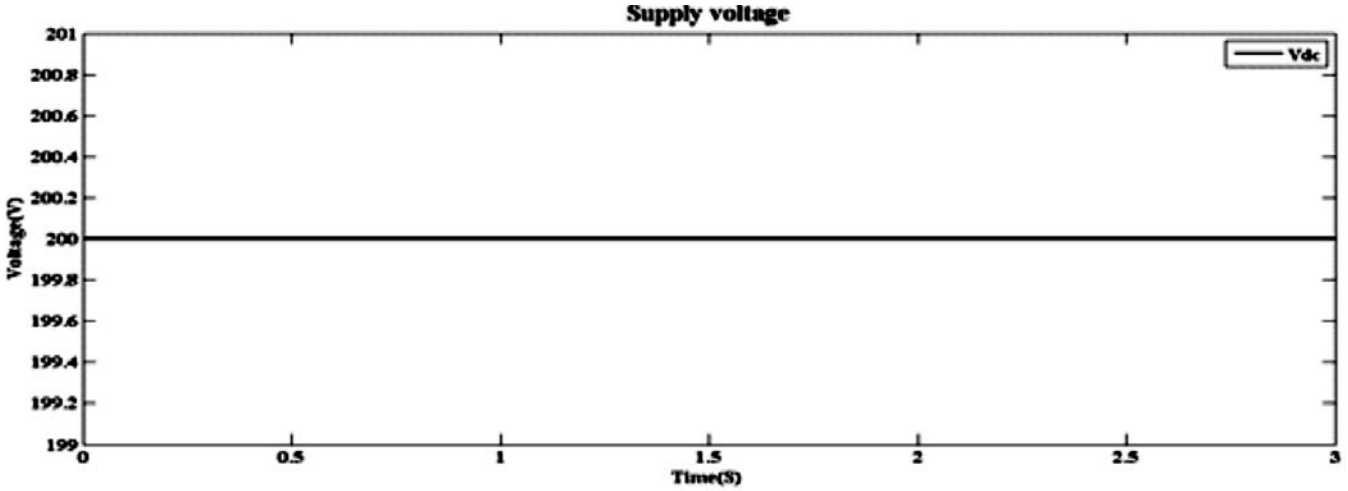


Fig. 12. Input dc voltage.

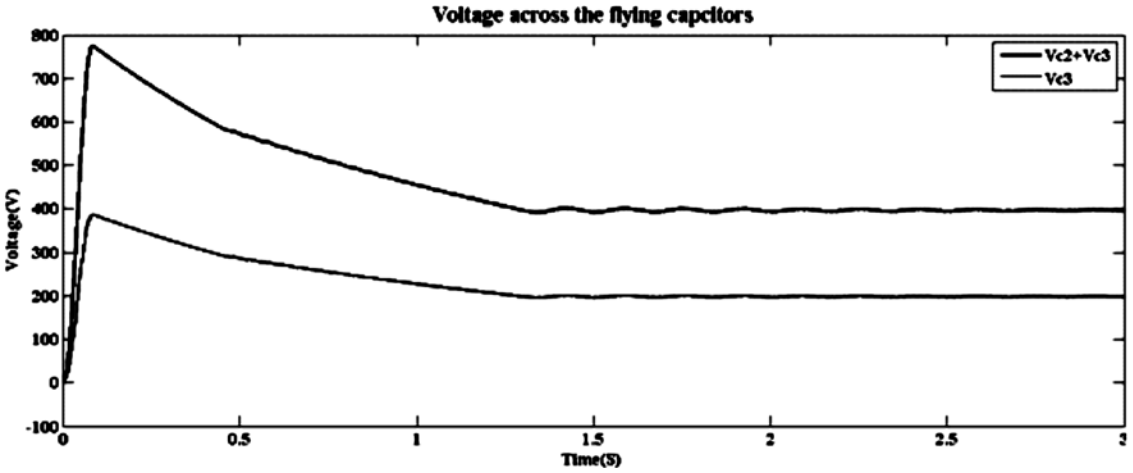


Fig. 13. Equal voltage distribution across the two flying capacitors in Five-level inverter.

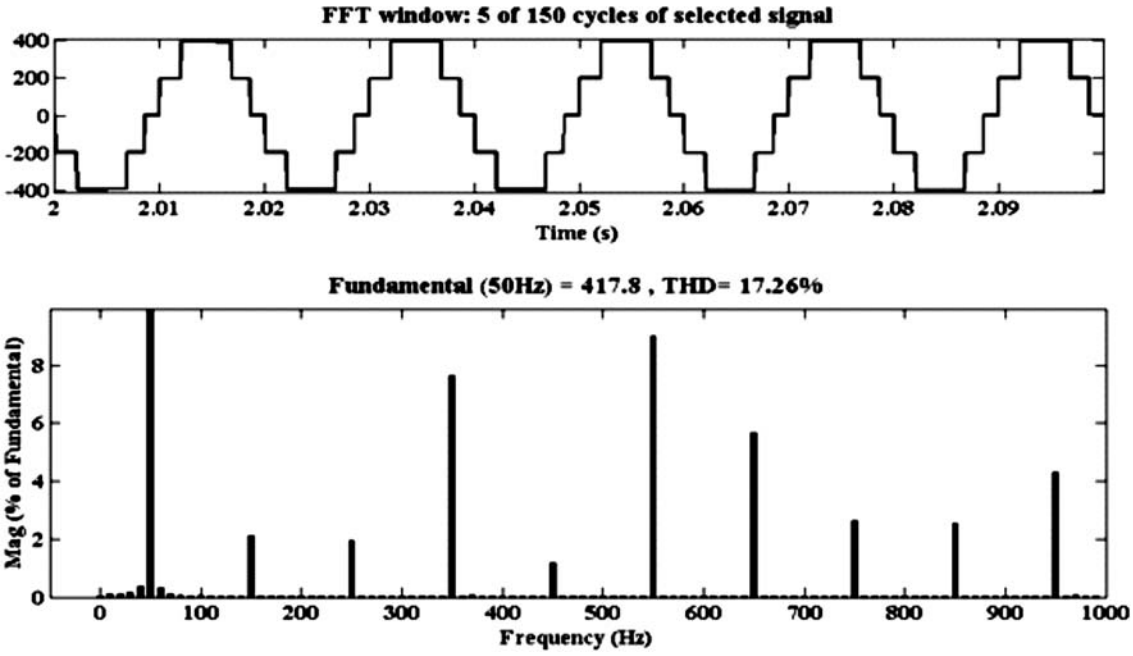


Fig. 14 (*a*). Output voltage and (*b*) THD spectrum of new five-level inverter with capacitor balancing circuit.

4. Z SOURCE BASED MLI WITH SINGLE IMPEDANCE NETWORK

4.1. Structure of an Inverter

Fig.15 shows the proposed circuit. It consists of impedance network with the switch Ssh along with the capacitor balancing circuit, level generator and H-bridge unit. The impedance network with switch Ssh is used for boost operation and the working of remaining sections is discussed in the previous topic. The novel impedance source multilevel inverters are reported in [23] and [24]. In [23], the inverter is capable of performing both buck-boost operations with a single impedance network but it contains same number of switching devices as that of conventional MLI's. In [24], a new multilevel structure has proposed with less number of switches, but it requires (*n*-1)/2 sources and independent impedance network across each source. This leads to increase in size and cost of inverter.

The proposed inverter shown in fig.15 is capable of providing the constant boost of 2 times the input voltage across the Z-source network without any shoot through *i.e.*, it works as the inverter shown in fig.9. If further boost is required the shoot through period is controlled by turning on switch S_{sh}. The proposed

inverter shown in fig.15 consists of one dc source, '*n*' capacitors including $\frac{(n-3)}{2}$ dc link capacitors, $\frac{(n-1)}{2}$ flying capacitors and two symmetrical capacitors in impedance network, and $\frac{n+9}{2}$ controlling switches that includes $\frac{(n-1)}{2}$ level generating switches, 4 switches of H-bridge and one switch S_{sh} to insert shoot through.

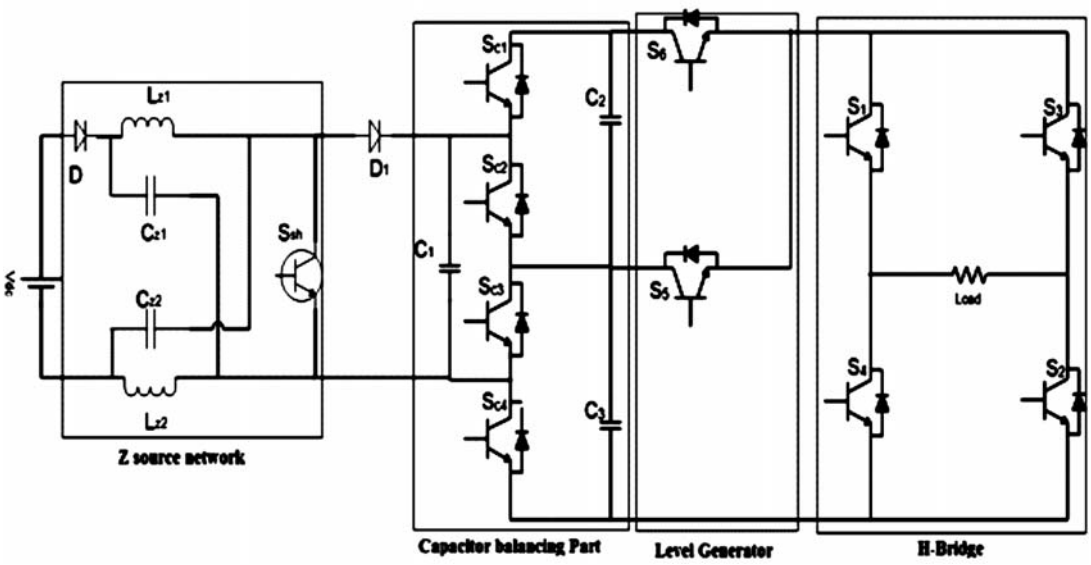


Fig. 15. Z-source five-level inverter with single impedance network.

The equations for the boost factor, voltage across the dc link and voltage across the impedance network are given by the equations (9), (10) and (11).

$$\text{Boost factor, B} = \frac{1}{1-\frac{2\sqrt{2}\times T_{sh}}{T}} \tag{9}$$

dc link voltage, $$V_{\text{dc link}} = 2 \times V_{dci} \tag{10}$$

Voltage across impedance network,

$$V_{dci} = B \times V_{dc} \tag{11}$$

Table 2. Wwitching procedure for Z-source MLI with single impedance network

Output Level	*Conducting switches*
2	S_1, S_2, S_6, Group2 switches
1	S_1, S_2, S_5, Group1 switches
0	S_2 and S_4
	S_1 and S_3
–1	S_3, S_4, S_5, Group2 switches
–2	S_3, S_4, S_6, Group1 switches
Shoot through state	S_{sh}
	S_{c2} and S_{c3}

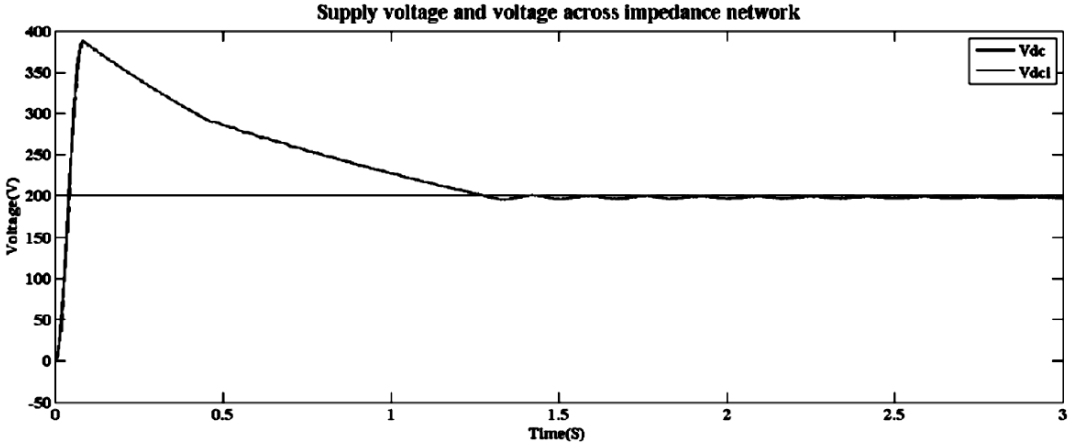
The switching pattern used for the Z source MLI inverter with single impedance network to obtain the positive and negative voltage in the output and the generation of the shoot through pulses are given in table. 2. If possible, the shoot-through pulses can also be generated and inserted in the circuit by turning ON the switches S_{c2} and S_{c3} instead of using the extra switch S_{sh}.

5. SIMULATION RESULTS

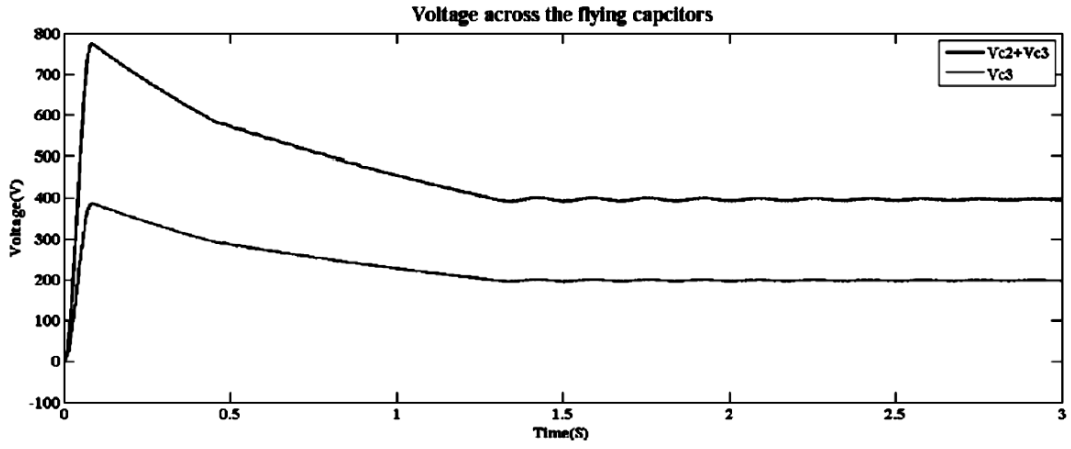
In order to verify the theoretical analysis results, MATLAB/SIMULINK package with simple boost control method is applied for the proposed inverter. The simulation parameters are as follows: input DC voltage 200 V; capacitance of capacitor used in impedance network and switched capacitor is 10 mF; inductance of a inductor used in impedance network 10mH; switching frequency for Sc1 to Sc4 and S1 to S6 is 50 Hz, switching frequency for Ssh is 10KHz and load impedance is 50 Ohms.

The figures 16, 17 and 18 shows the simulation results of the Z source five level inverter with single impedance network with three different booting factors such as B = 1, 2 and 3. The figures 16(*a*), 17 (*a*) and 18 (*a*) shows the simulated waveforms of the input voltage and the voltage across the impedance network, the figures 16 (*b*), 17 (*b*) and 18 (*b*) shows the simulated waveforms of the balanced voltage across the flying capacitors C_2 & C_3, the figures 16 (*c*), 17 (*c*) and 18 (*c*) shows the simulated waveforms of the single phase output voltage and the figures 16 (*d*), 17 (*d*) and 18 (*d*) shows the THD spectrum with three T_{sh} periods or three boost factors when input is given across the dc link capacitor C_1 (Fig.9).

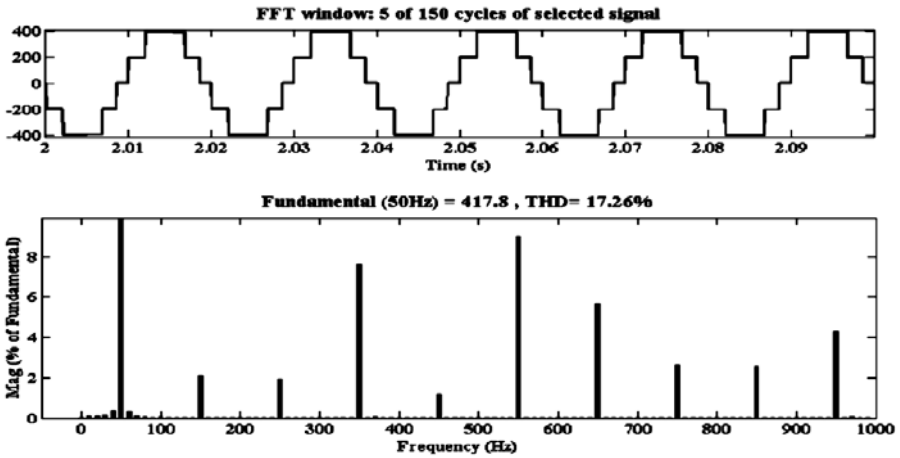
In fig.16, the output voltage across the inverter is boosted to 2 times the input without inserting any shoot-through period and this is due to balanced capacitor circuit. This is not possible with conventional inverter or conventional ZSI.



16 (a)

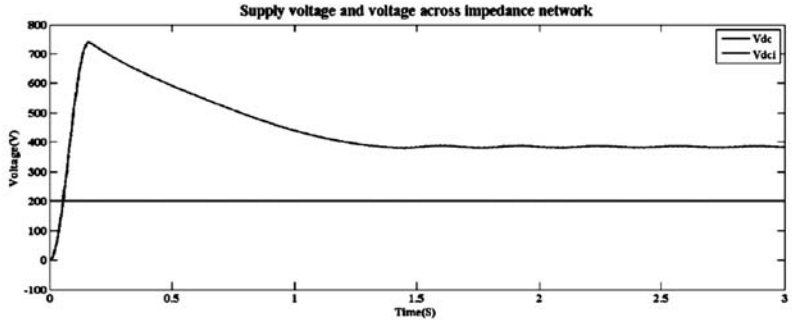


16 (b)

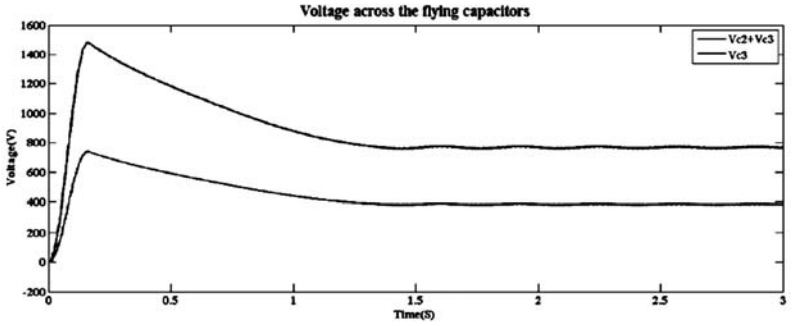


16 (c) & (d)

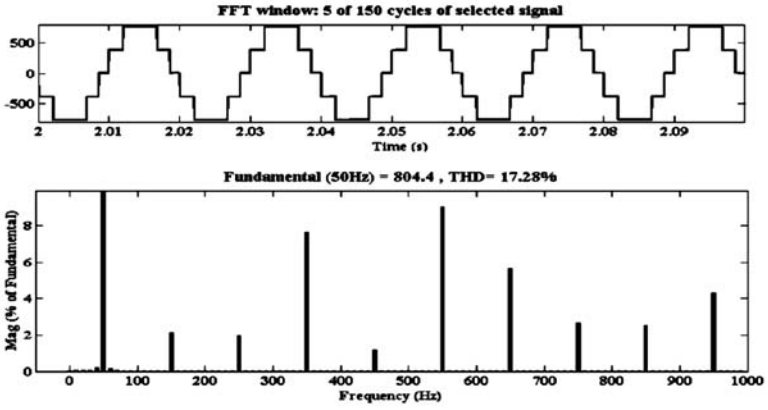
Fig. 16. (*a*) Voltage across the input and impedance source network, (*b*) voltage across the flying capacitors, (*c*) output voltage and (*d*) THD spectrum with B = 1



17(a)

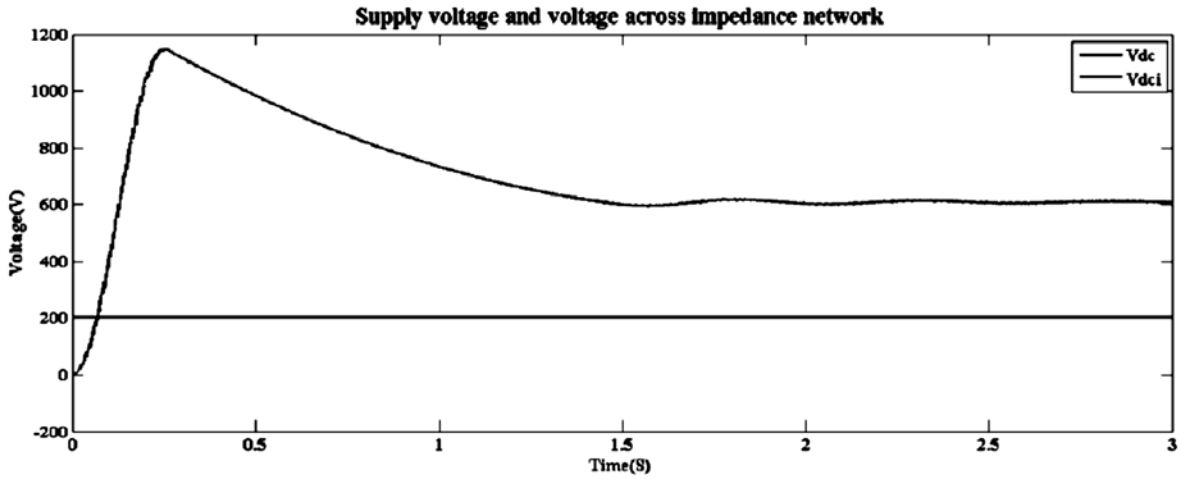


17(b)

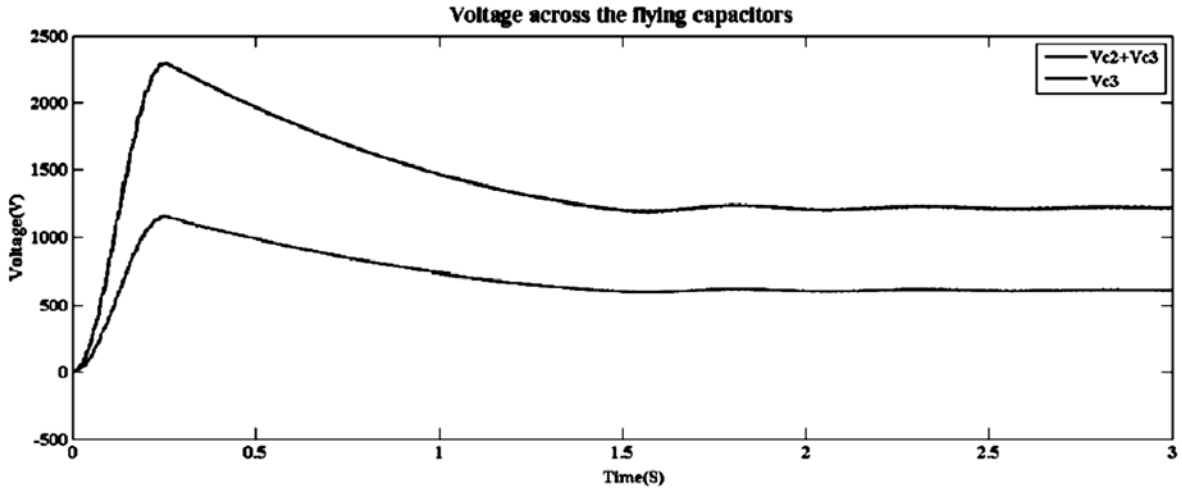


17 (c) & (d)

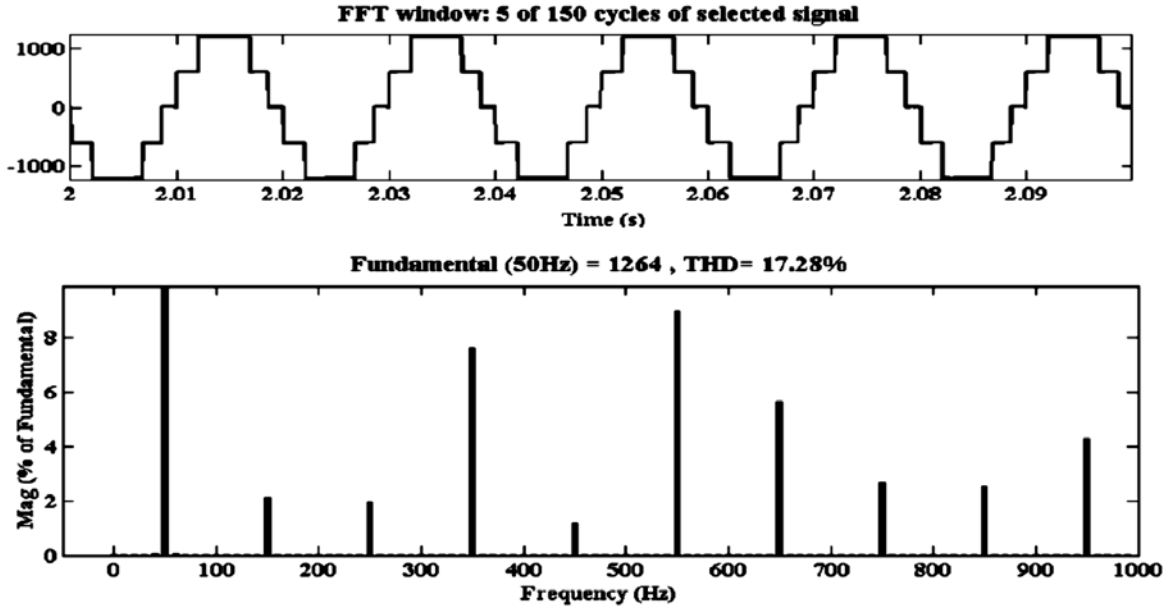
Fig. 17. (*a*) Voltage across the input and impedance source network, (*b*) voltage across the flying capacitors, (*c*) output voltage and (*d*) THD spectrum with B = 2



18(a)



18(b)



18(c) & (d)

Fig. 18. (*a*) Voltage across the input and impedance source network, (*b*) voltage across the flying capacitors, (*c*) output voltage and (*d*) THD spectrum with B = 3

Table. 3. Boost factor Vs fundamental voltage & THD in Proposed Z-source Five-level inverter.

Boost factor (B)	*Fundamental voltage (Vo)*	*%THD*
1.	417.8	17.26%
2.	804.4	17.28%
3.	1264	17.28%

6. CONCLUSION

This paper presents a novel Z Source based Balancing Capacitor Multi level Inverter with single impedance network. The proposed inverter is capable of providing constant boost of 2 times the input voltage and additional boost is obtained by adding shoot trough states for normal pulses. Fundamental output is greater than the conventional and recently proposed inverter. Also, the THD is maintained nearly constant for different boost factor.

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