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Improving Power Quality of Renewable Energy Source by Using UPQC Based on Cascaded Multilevel Topology

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Abstract: In Renewable energy source, power quality was very essential factor in the power transmission area. Power quality is protecting all electrical and electronic components in various fields of instruments like medical, industrial, household applications and controlling instruments. A technique is achieving to make constant parameters at deviation of load side such as magnitude of real and reactive power, magnitude of voltage and current fluctuation and power factor correction by UPQC. In this paper we have concentrate to improve good power factor, stability of supply voltage variations, harmonics reduction, etc. this technique construct by DVR, DSTATCOM, cascaded multilevel inverter and DC-link capacitor. The power quality problem such as SAG-SWELL through a three phase Unified Power Quality Conditioner (UPQC) under unbalanced and distorted load conditions. it can be overcome power quality problems at the point of common coupling on transmission network (distribution system) under unbalanced and distorted load conditions.

Keywords: UPQC (Unified Power Quality Conditioner), PCC (Point of Common Coupling), THD (Total Harmonic Distortion), APF (Active Power Filter), EMI (Electro Magnetic Interference), CPWM (Cascaded Pulse Width Modulation).

1. INTRODUCTION

The modern power electronics and digital control technology of renewable energy sources are rise to connect in the distribution systems. In general voltage fluctuation is affecting the power quality (PQ), sag-swell problems are involving in the transmission section, because of the nonlinear loads and unbalanced loads have degraded in the power distribution network. A custom power device has been expected for enhancing the quality and reliability of electrical transmitting power.

Unified PQ conditioner (UPQC) is used to protect the electrical and electronic goods which consist of series & shunt inverters connected back-to-back in transmission line and deals with unbalance of voltage & current. Simultaneously UPQC can act as shunt and series active power filters. The series active filter of UPQC is called as dynamic voltage restorer (DVR). It can maintain the output voltage constant to the load deviation. The shunt active filter of UPQC is called as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power. The voltage and current phase difference is nil means it make unit power factor. Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter.

2. LITERATURE REVIEW

The various types of pulse width modulation (PWM) controlled methods are explained in this paper such as Single-pulse modulation, Sinusoidal pulse width modulation (Carrier based Pulse Width Modulation Technique)

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and Multiple pulse modulation. space vector pulse width modulation (SVPWM) technique is improves the quality of the current and reduce the torque ripple in induction motor drive while maintaining the other performance characteristics of the system.[1] The DC-Link voltage balancing capability of the method used to maintain power quality in each H-bridge and simplifying the control structure. [2]. In another proposed topology helps to match the shunt and series active filters of the UPQC. It is combination of capacitor and inductor circuit active filter, the neutral point is connected with DC-link voltage, it is avoid fourth terminal in voltage source inverter. So that switching frequency reduced.[3]-[5] a UPQC with cascaded multilevel inverter is proposed to reduce voltage sag problems, unbalance and load power factor in transmission distribution system by multilevel UPQC. In this technique transformer is replaced by UPQC applied and it is one of its advantages.[6]-[10]. In another one discusses the control strategy of the UPQC with a focus on the flow of instantaneous real power and reactive power inside there are limitations on the rating and a phase difference for the voltage sag effectively and economically by using minimum active power.[11]-[13].

3. PROPOSED SYSTEM

In this topology, the system neutral point has been connected to the negative terminal of the dc bus along with the feedback capacitor C_f in series with inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor Cf has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load.

The addition of capacitor in series with inductor of the shunt active filter will reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. It is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application, and the reactive power compensation is not considered, which is an important aspect in UPQC applications. In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC. It also has the capability of compensating the voltage sag/swell as well as voltage regulation and harmonic compensation at the Point of Common Coupling. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing.

In, four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in existing system a T connected transformer and three-phase VSC based DSTATCOM is used. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer. In this paper, a UPQC topology with reduced dc-link voltage is proposed. This topology consists of capacitor in series with the interfacing inductor of the shunt active filter and it minimized size, cost and hence to reduce the overall harmonics of the transmission network.

3.1. Unified Power Quality Conditioner

The general block diagram of UPQC is shown in figure 1 here UPQC is connected between source and load. There are two inverters, one is series and other is shunt inverter. The inductance and capacitance is connected with the series inverter. In between the shunt and series converter dc link capacitor is used.

The DC source may be Battery or fuel cell or rectified from AC source. The series inverter converts AC supply to DC output. This converter is used to eliminate volatge variation of the line supply. The reactive power is controlled by this converter. The shunt inverter converts DC supply to AC output. This converter is used to eliminate a selective harmonics in the line current.the inverter output is injected through shunt transformer into line. Inverter has

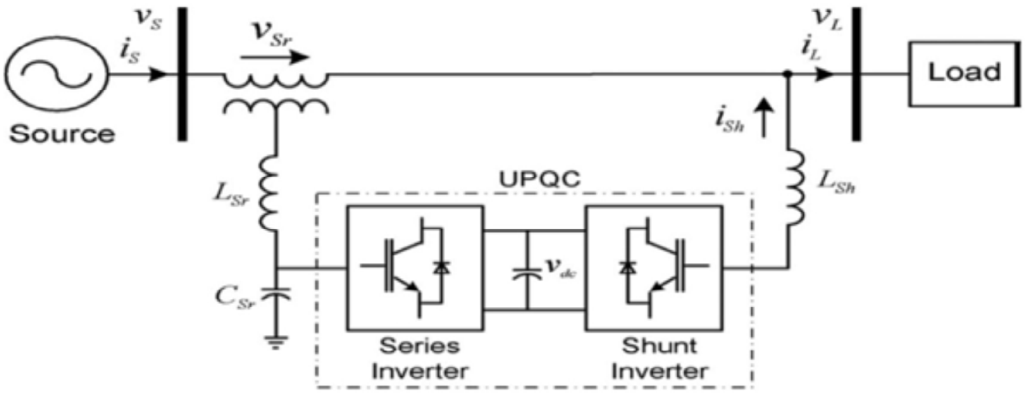


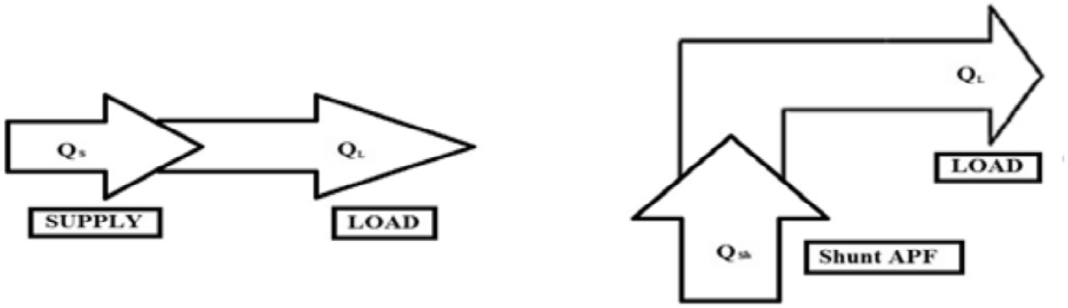
Figure 1: Basic Block Diagram of UPQC

more harmonics it should be removed with help of LC filter circuit. It gives the AC supply to rectifier. The input side having one inductive filter. It is used to improve the input power factor. Cascded Multilevel inverter is to generate ac output voltage it is used to run ac motor and any appliance required for ac voltage.

3.1.1. Operating Principle of Upqc

In normal condition, the reactive power did not affect to the load side because of unified power flow through the entire section. Its shown on figure 2(a). The shunt active filter is activated on unified power quality condition. The reactive power flow during the entire operation of unified power quality conditioner is shown in the Figure 2(b).

The voltage sag is occur in the condition of $k < 0$ and the terminal voltage is less than load voltage ($V_T < V_L$), If PSR is positive cycle means power flow through the active filter to the load. At the time of sag, flow of power is less than the normal rated power. Thus we can say that the required active power is taken from the utility itself by taking



(a) without UPQC **(b) with shunt APF**

Figure 2: Overall Reactive Power Flow

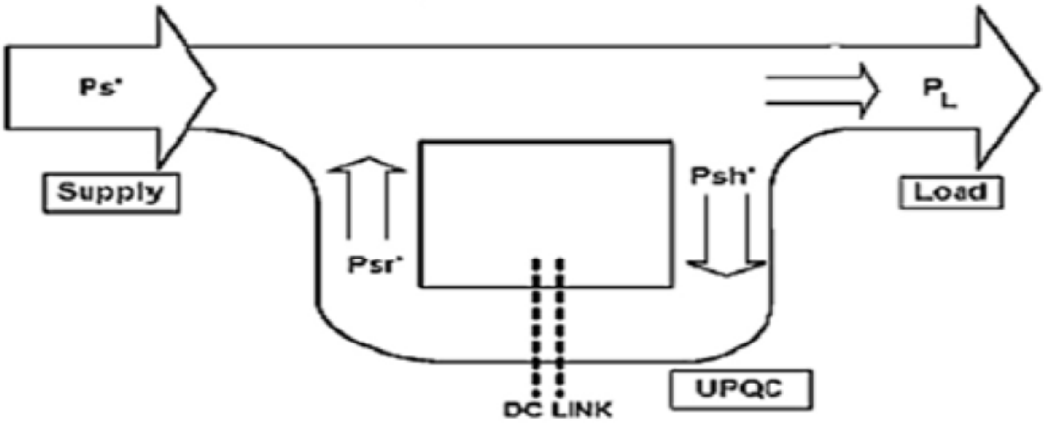


Figure 3: Overall Active Power Flow during Sag Condition

more current so as to maintain the power balance in the network and to keep the dc link voltage at desired level Ps'-source power travel to the load on during voltage sag condition, *Psr*'-series injected power by APF. The sum of source power and injected series power is needed to compensate load power (*Ps″+ Psr″*) during sag period and to maintain the normal working condition. Psh' - power absorbed by shunt APF during voltage sag condition. The output of the series and shunt inverter power is equal. *Psr'= Psh'* The overall active power flow during sag condition is shown in Figure 3.

The voltage swell is occur in the condition of k > 0 and the terminal voltage is greater than load voltage ($V_T > V_L$), If PSR is negative cycle means power flow through the active filter and load. At the time of swell, flow of power is greater than the normal rated power. Thus we can say that the required active power is taken from the utility itself by taking more current so as to maintain the power balance in the network and to keep the dc link voltage at desired level

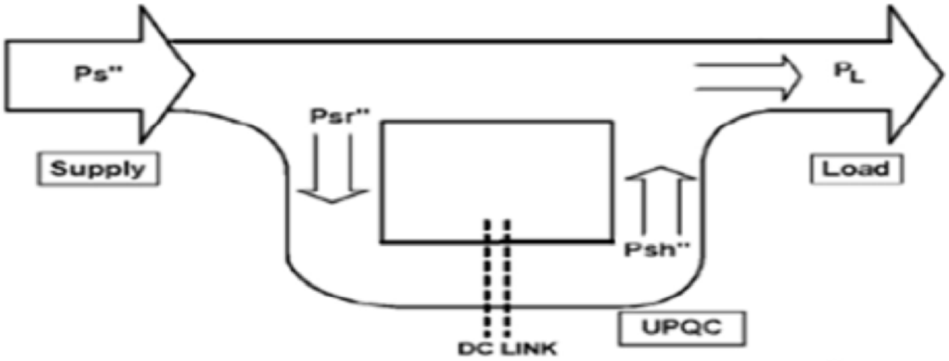


Figure 4: Overall Active Power Flow during Swell Condition

Ps'-source power travel to the load on during voltage swell condition. Psr'-series injected power by APF. The difference of source power and injected shunt power is needed to compensate load power (*Ps″- Psr″*) during swell period and to maintain the normal working condition. *Psh*' - power absorbed by shunt APF during voltage swell condition. Consequently the output of series and shunt inverter power is equal (*Psr'= Psh'*). The overall active power flow during swell condition is shown in Figure 4.

If the condition is $k = 0$ and $V_T = V_L$, means there will not be any real power exchange through unified power quality conditioner. This is the normal operating condition. The overall active power flow is shown in Figure 5

Ps-power supplied by the source to the load during voltage swell condition. Psr-power injected by series APF in such a way that sum *Ps*" = *Psr*" will be the required load power during normal working condition. *Psh* - power delivered by shunt APF during voltage sag condition. Consequently the output of series and shunt inverter power is equal (*Psr* = *Psh*).

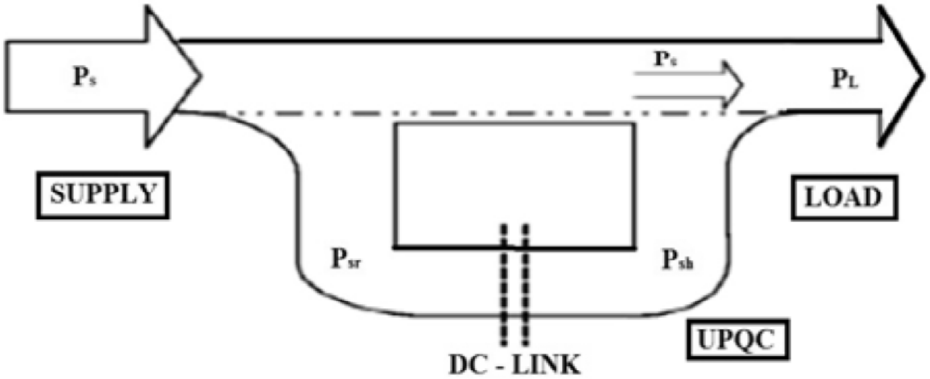


Figure 5: Active Power Flow during Normal Working Condition

3.2. DSTATCOM

A DSTATCOM is a reactive power compensating device which can either inject or absorb reactive power on the transmission line it consists of Voltage Source Converter (VSC) along with a DC link capacitor as shown in figure 6.

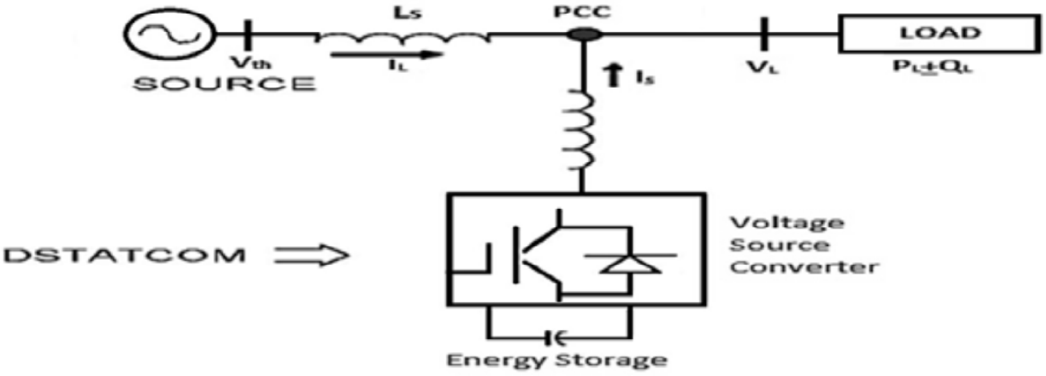


Figure 6: Basic structure of DSTATCOM

If the output voltage of VSC is equal to AC terminal voltage. It generate reactive power whereas if VSC voltage is greater than terminal voltage it can absorb reactive power. By using D-STATCOM, the power factor correction is also employed. So with the usage of DSTATCOM to make the voltage & current inphase with each other and to make voltage regulation is improved and to become power factor as unity.

The shunt injected current I_{sh} can be written as,

$$I_{sh} = I_L - I_S = I_L - \frac{(V_T - V_L)}{Z_T} \tag{1}$$

$$I_{sh} \angle \eta = I_L \angle \phi \tag{2}$$

The complex power injection of the D-STATCOM can be expressed as

$$S_{sh} = V_L I_{sh}^{*} \tag{3}$$

Where,

I_{sh} – Shunt injected current

Z_T – System impedance

S_{sh} – Complex Power

4. SAG and SWELL fault

The basic transmission network structure as shown in figure 7 This is the general view from generating station to load, which has a transmission line of 100 kilometer. Here we are creating a Sag & Swell fault manually at the time period of 0.3 to 0.5 seconds & time period of 0.7 to 0.9 seconds by closing the Phase A. the sag parameter changed in simulation of MATLAB and its shown in figure 8 and the swell parameter changed in simulation of MATLAB and its shown in figure 9. After execute of simulation result the output of voltage and current waveform is shown in figure 10, here in between duration of 0.3 to 0.5 & 0.7 to 0.9 sec have more fluctuation in the voltage and currents wave forms. Simulation graph of the magnitude of voltage and current at fault occur area is clearly intimate in Figure 11. And how the real power and reactive power gets distorted at the Sag-swell Fault time period, is noticed in figure 12. Then the Total Harmonic Distortion has measured the duration of sag-swell fault occur in the transmission line. The percentage of THD is very large amount of percentage (58.79%) present. This will be rectified using the unique device called as UPQC as mentioned in figure 13. The above faults are rectifying by our proposed method. The general simulation diagram of our proposed is shown in figure 14. The eleven level cascaded multilevel inverter inject to the active and reactive filter components. This Eleven level inverter used in the both DVR and DSTATCOM and its shown in figure 15 and corresponding output wave form is shown in figure 16. Then Simulation circuit diagram of Phase Opposition Disposition PWM is shown in figure 17. This PWM technique used in our circuit and rectify the sag-swell problem. These rectified output voltage and current at the time of Sag-swell Fault shown in figure 18. We can see that the distortion in the time period from 0.3 second to 0.5 second due to the Sag fault has been compensated by using UPQC similarly 0.7 to 0.9 sec swell fault also rectified by our proposed method. The Magnitude wave form of voltage and current is shown in figure 19, simultaneously we have measured the magnitude wave form of real power and reactive power injects at faulted area illustrated in Figure 20.After using our proposed system of UPQC in the Transmission line and analyzing the Total Harmonic Distortion we can found that the harmonic level in the Transmission line has been reduced to 1.66% as shown in figure 21.

4.1. Simulation of SAG-SWELL Fault occur without UPQC

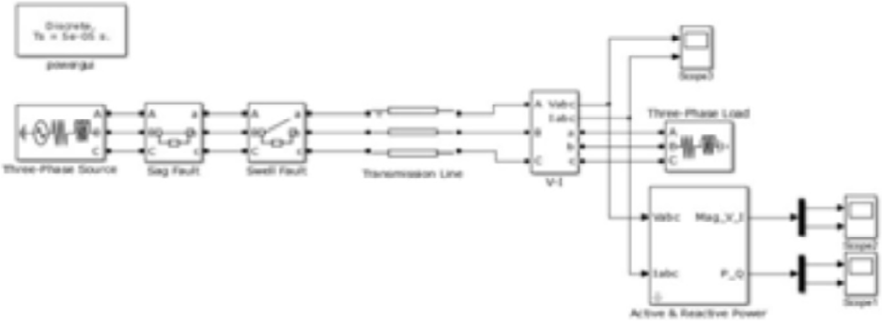
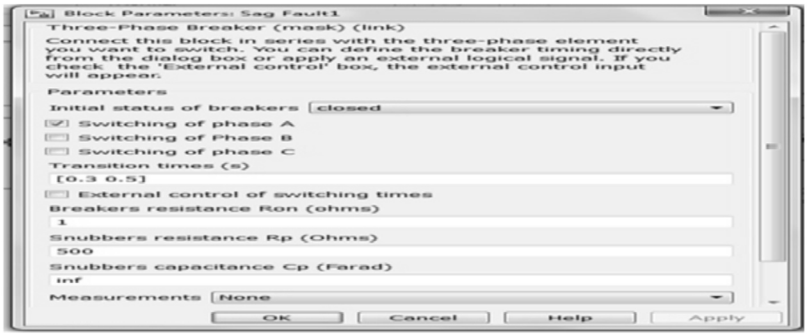


Figure 7: Simulation circuit diagram of Sag & swell Fault occur without UPQC

4.2. Single Line Sag Fault


Block Parameters: Sag Fault1

Three-Phase Breaker (mask) (link)

Connect this block in series with the three-phase element you want to switch. You can define the breaker timing directly from the dialog box or apply an external logical signal. If you check the 'External control' box, the external control input will appear.

Parameters

Initial status of breakers: closed

☑ Switching of phase A

☐ Switching of Phase B

☐ Switching of phase C

Transition times (s): [0.3 0.5]

☐ External control of switching times

Breakers resistance Ron (ohms): 1

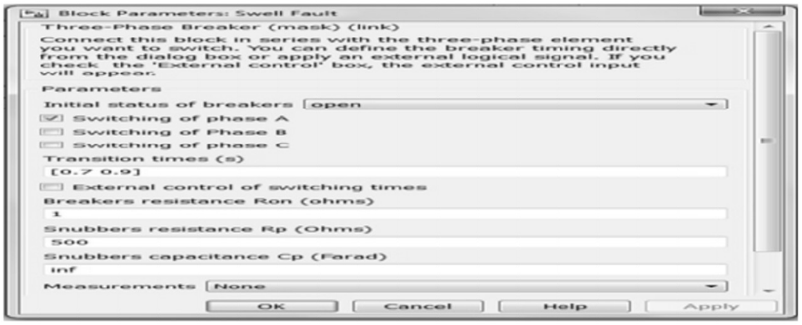
Snubbers resistance Rp (Ohms): 500

Snubbers capacitance Cp (Farad): inf

Measurements: None

Figure 8: Simulation parameter of single line sag fault

4.3. Single line Swell Fault


Block Parameters: Swell Fault

Three-Phase Breaker (mask) (link)

Connect this block in series with the three-phase element you want to switch. You can define the breaker timing directly from the dialog box or apply an external logical signal. If you check the 'External control' box, the external control input will appear.

Parameters

Initial status of breakers: open

☑ Switching of phase A

☐ Switching of Phase B

☐ Switching of phase C

Transition times (s): [0.7 0.9]

☐ External control of switching times

Breakers resistance Ron (ohms): 1

Snubbers resistance Rp (Ohms): 500

Snubbers capacitance Cp (Farad): inf

Measurements: None

Figure 9: Simulation parameter of single line swell fault

4.4. Output Voltage and Current under Single Phase Fault Without UPQC

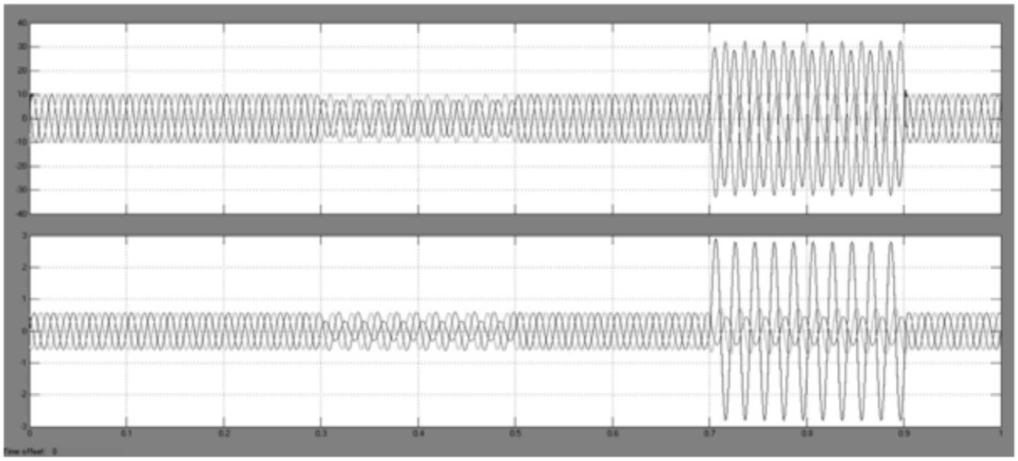


Figure 10: Simulation circuit diagram of Output Voltage and Current under Single Phase Fault Without UPQC

4.5. Magnitude wave form of Voltage and Current at Fault Condition

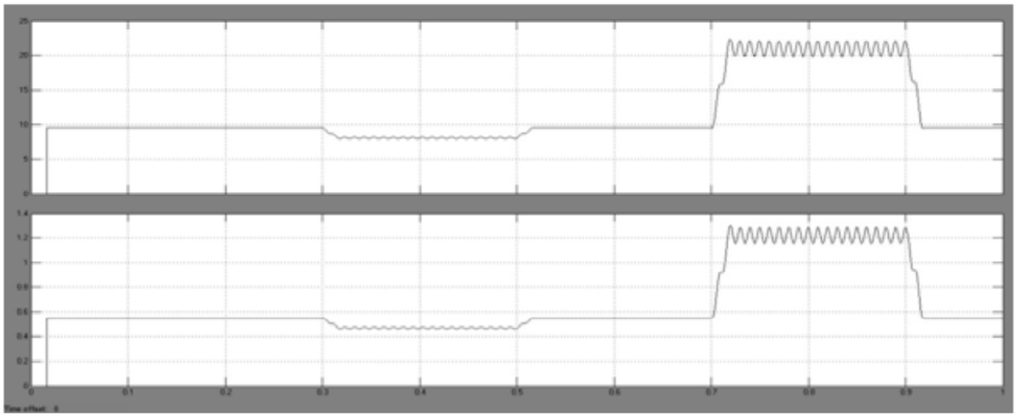


Figure 11: Simulation graph of Voltage and Current at Fault Condition

4.6. Real Power and Reactive Power at Fault Condition Without UPQC

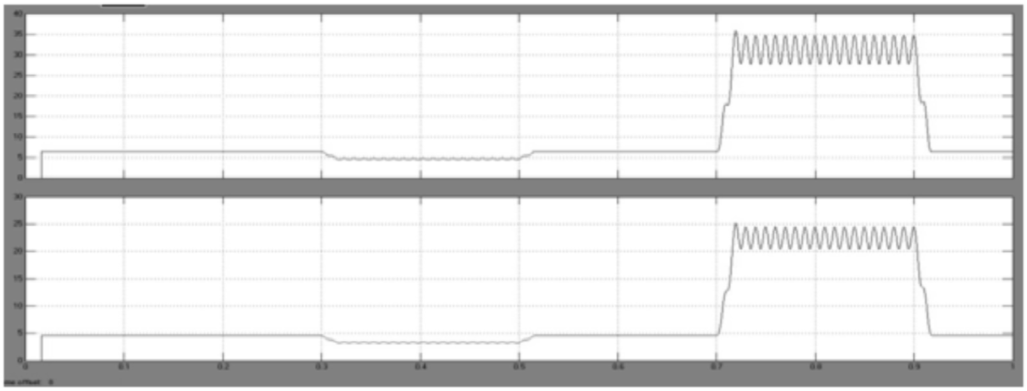
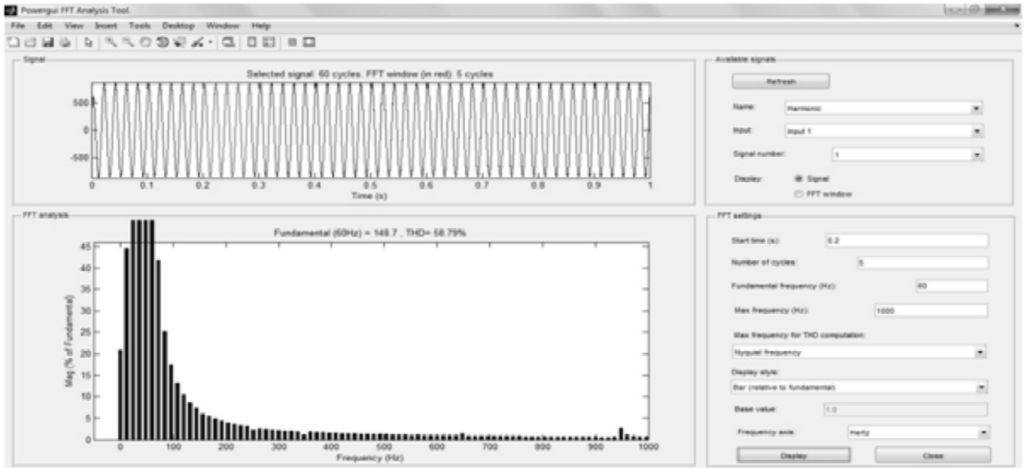


Figure 12: Simulation graph of Real Power and Reactive Power at Fault Condition Without UPQC

4.7. THD Analysis at Fault Condition



Selected signal: 60 cycles. FFT window (in red): 5 cycles

Fundamental (60Hz) = 148.7 , THD= 58.79%

Available signals

Name: Harmonic

Input: input 1

Signal number: 1

Display: ● Signal ○ FFT window

FFT settings

Start time (s): 0.2

Number of cycles: 5

Fundamental frequency (Hz): 60

Max frequency (Hz): 1000

Max frequency for THD computation: Nyquist frequency

Display style: Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Figure 13: THD Analysis at Fault Condition

4.8. Simulation of Rectifying the SAG-SWELL Fault with UPQC circuit

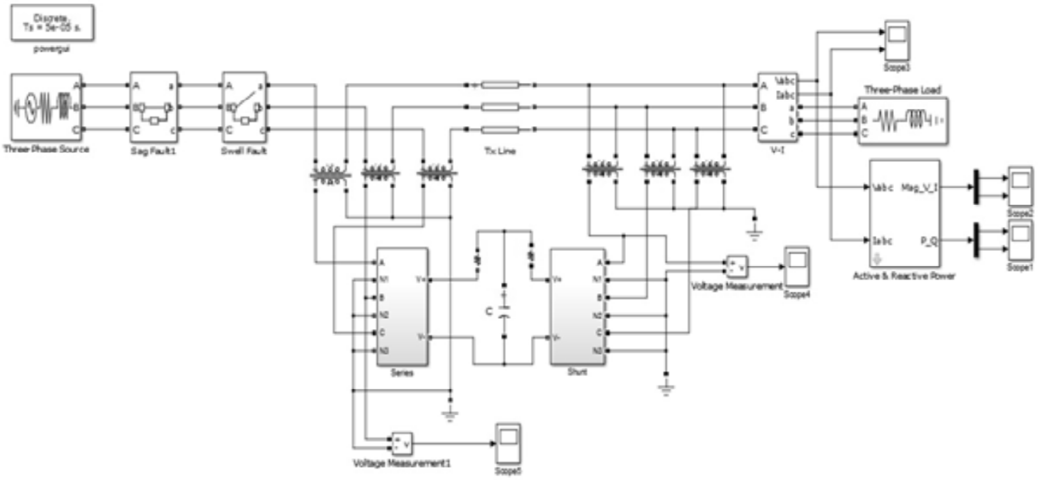


Figure 14: Simulation of Rectifying the Sag-swell Fault With UPQC circuit

4.9. Eleven Level Inverter

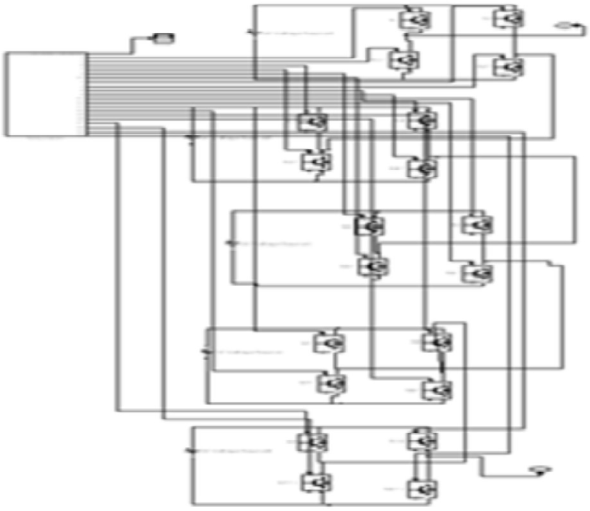


Figure 15: Simulation of Eleven Level cascaded multilevel

4.10. Eleven Level Output

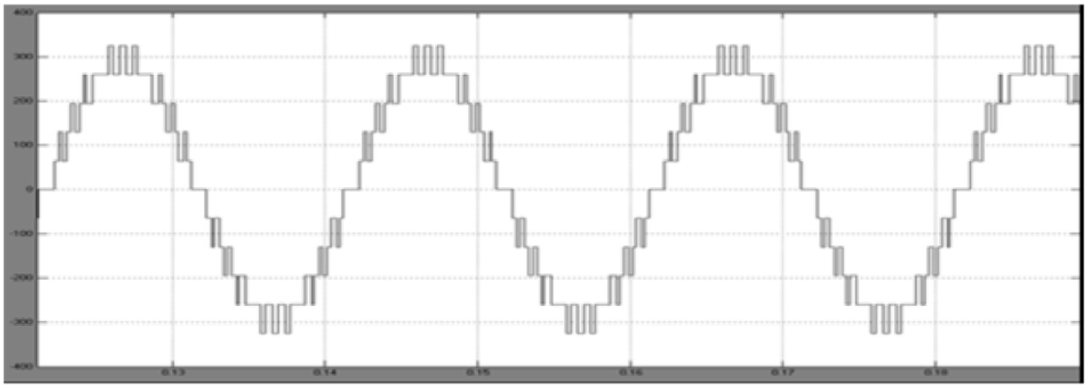


Figure 16: Simulation of Eleven Level cascaded multilevel output waveform

4.11. Phase Opposition Disposition PWM

Figure 17: Simulation circuit diagram of Phase Opposition Disposition PWM

4.12. Output Voltage and Current Injects at Fault Condition

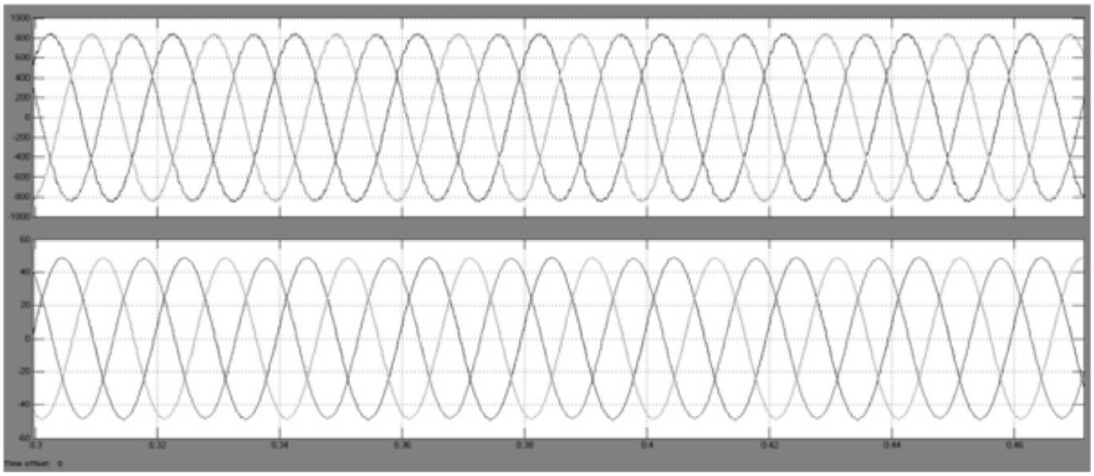


Figure 18: Simulation Output Voltage and Current Injects at Fault Condition waveform

4.13. Magnitude wave form Voltage and Current

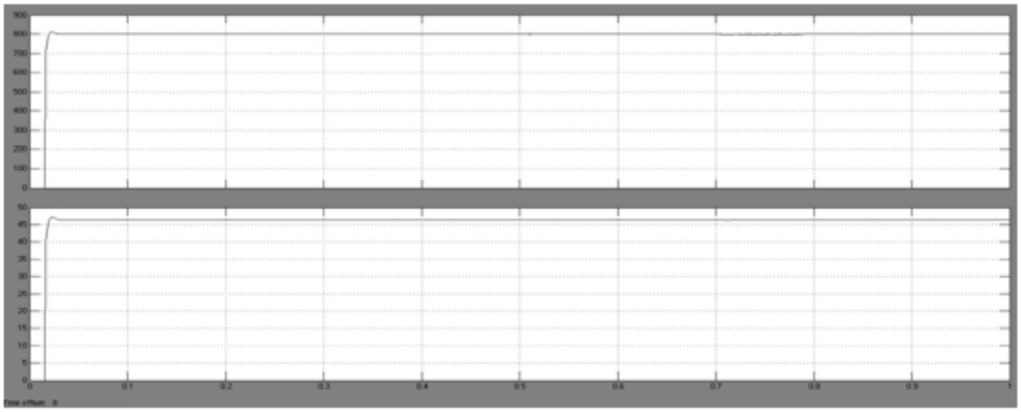


Figure 19: Simulation Magnitude wave form of voltage and Current

4.14. Real Power and Reactive Power Injects at Fault Condition

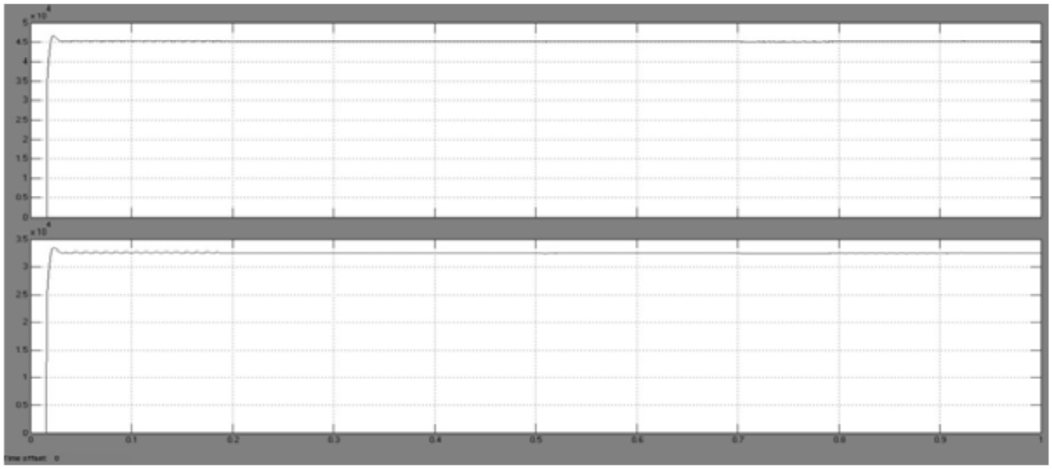
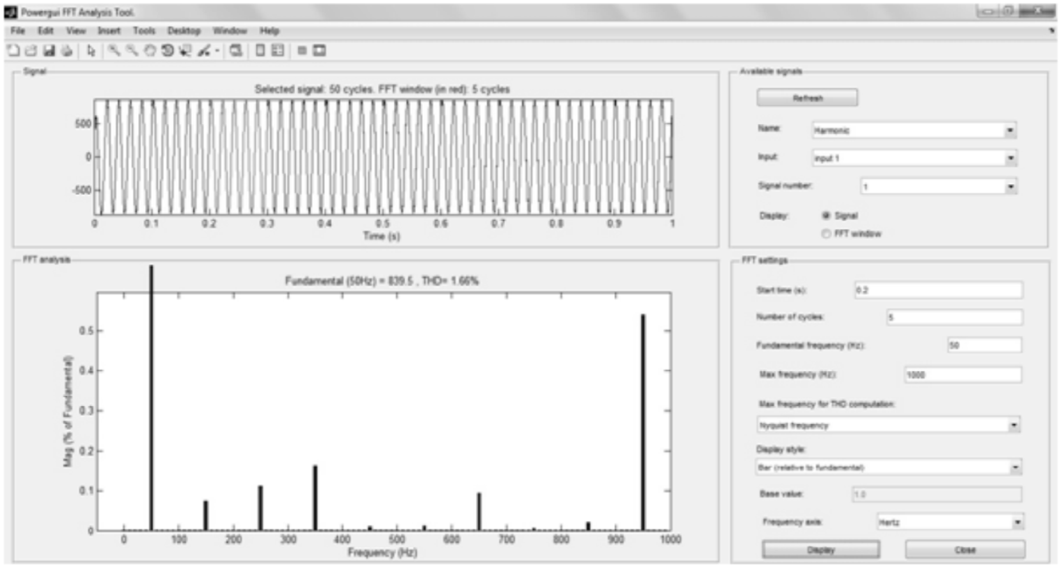


Figure 20: Simulation wave form of Real Power and Reactive Power Injects at Fault Condition

4.15. THD Analysis Using UPQC



Selected signal: 50 cycles. FFT window (in red): 5 cycles

Name: Harmonic
Input: input 1
Signal number: 1
Display: ● Signal ○ FFT window

Fundamental (50Hz) = 839.5 , THD= 1.66%

Start time (s): 0.2
Number of cycles: 5
Fundamental frequency (Hz): 50
Max frequency (Hz): 1000
Max frequency for THD computation: Nyquist frequency
Display style: Bar (relative to fundamental)
Base value: 1.0
Frequency axis: Hertz

Figure 21: Simulation view of THD Analysis Using UPQC

5. CONCLUSION

A modified UPQC topology for DVR & DSTATCOM system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non-stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed cascaded multilevel inverter based UPQC topology with reduced dc-link voltage and it consists of capacitor in series with the interfacing inductor of the shunt active filter and hence to reduce the cost, bulkiness and overall harmonics of the transmission network. From the study, it is found that the modified topology has less average switching frequency, less THDs from 58.79% to 1.66% in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

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