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Transformerless, 11-level DC/AC hybrid topology with quasi z source network based on single dc source, for photo voltaic applications

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ABSTRACT

This paper introduces a novel transformer less multilevel hybrid conversion topology, which presents as the most important contribution to the generation of a single isolated DC voltage source without transformers, for applications in DC/AC cascade hybrid multilevel converters. This is achieved by modifying the traditional DC/DC Buck converter topology. A suitable switching strategy is employed to regulate the isolated DC voltage source at the flying capacitors. Furthermore, the simulation results obtained demonstrate the efficiency of the proposed inverter to ensure the required performance. The quasi Z source network is introduced for low ripples and high voltage at input source.

Keywords: Photo Voltaic (PV), Quasi Z Source (QZS), Quasi Source Inverter (QSI), Total Harmonic Distortion (THD), Voltage Source Inverter (VSI).

1. INTRODUCTION

Modernization on transmission and distribution grids require of the new systems based on power electronic converters, with favorable characteristics such as high efficiency, high power density, and low harmonic distortion, which suitable into the distributed generation and smart-gridconcepts[2]. Due to its characteristics, Grid-connected photovoltaic or wind generation systems represent the most widespread solution for residential renewable energy generation complied with the new tendencies in the electrical networks. Multilevel converters have gained widespread acceptance for applications in power grids of medium and high voltage. Some advantages of these converters are low harmonic distortion in the output voltage, low voltage stress on devices, low switching frequency which leads to better efficiency and also it can operate without magnetic elements [5]. Given these advantages, the multilevel converter is a power electronics area device under intensive investigation.

Multilevel converters were initially employed in high voltage grids and power train applications. The existing system is presented in Fig. 1. After time, this was introduced in renewable energy converters inside utility-scale plants, in which they are still largely employed[3]. In the proposed system we introduced a Quasi Z-Source (QZS) network to reduce maximum ripple content in the input source and to increase the input value.

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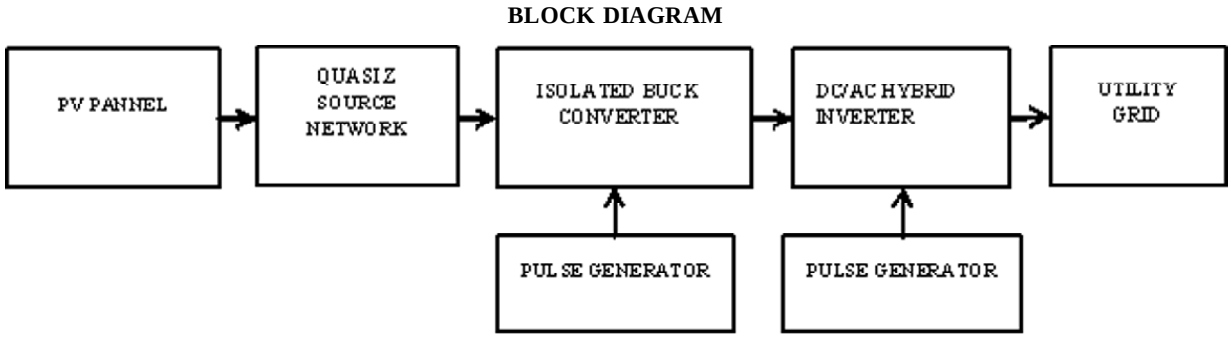

Figure 1: Block diagram of existing system

2. QZS NETWORK

The QZS circuit differs from that of a conventional ZS in the LC impedance network interface between the source and inverter. The unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state which is forbidden in traditional VSI. This network will effectively protect the circuit from damage when the shoot through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage.

The impedance network of QZS is a two port network. It consists of inductors and capacitors connected as shown in Fig.2.This network is employed to provide an impedance source, coupling the converter to the load. The dc source can be a battery, diode rectifier, thyristor converter or PV array.

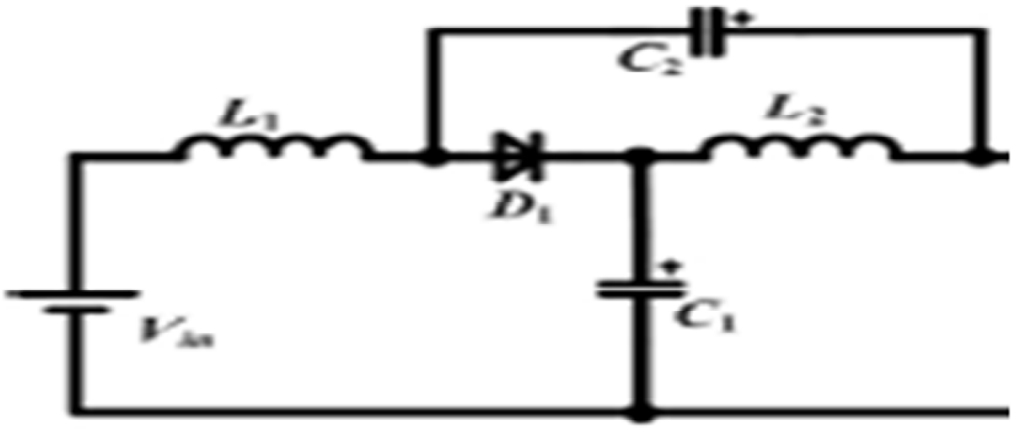

Figure 2: Quasi Z source

2.1. Operating Principle and Equivalent Circuit of QZS

The two modes of operation of a quasi z-source are,

(1) Non-shoot through mode (active mode).

(2) Shoot through mode.

2.2. Active Mode

In the non-shoot through mode, the switching pattern for the QZS is similar to that of a VSI. Active mode is shown in Fig.3. The inverter bridge, viewed from the DC side is equivalent to a current source. The input dc voltage is available as DC link voltage input to the inverter, which makes the QZS behave similar to a VSI [4].

2.3. Shoot Through Mode

In the shoot through mode, switches of the same phase in the inverter bridge are switched on simultaneously for a short duration. The source however does not get short circuited when attempted to do so because of the presence LC network, while boosting the output voltage [1]. The DC link voltage during the shoot through states, is boosted by a boost factor, whose value depends on the shoot through duty ratio for a given modulation index.

Hence QZS inherits all the advantages of the ZS. Fig.4 shows the QZS in shoot through mode. It can buck or boost a voltage with a given boost factor. It is able to handle a shoot through state, and therefore it is more reliable than the traditional VSI. It is unnecessary to add a dead band into control schemes, which reduces the output distortion. In addition, there are many unique merits of the QZS when compared to the ZS.

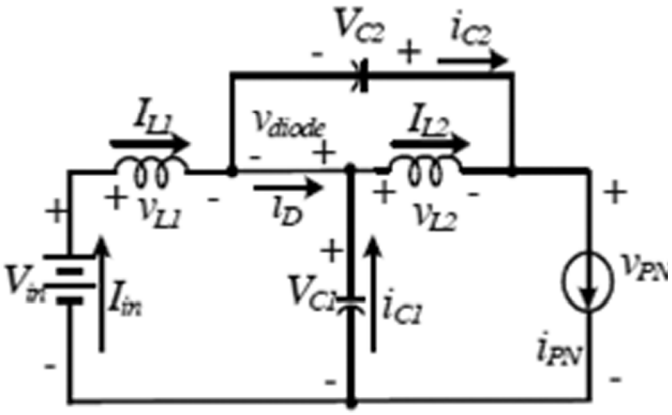

Figure 3: Equivalent circuit of QZSI in Active mode

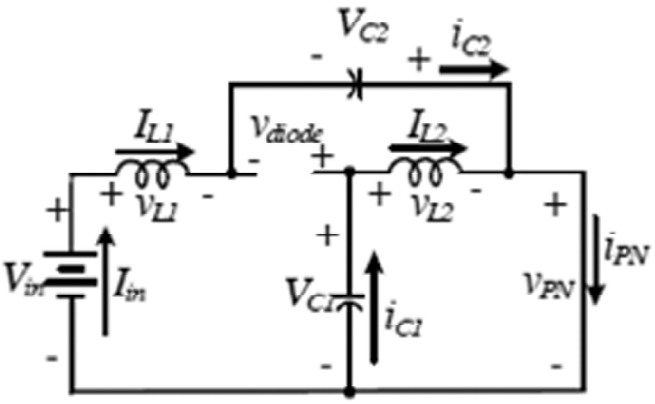

Figure 4: Equivalent circuit of QZS in Shoot through Mode

3. BUCK CONVERTER STEP-DOWN CONVERTER

In this Fig. 5 converter circuit the transistor turning ON will put voltage V_{in} on one end of the inductor. This voltage will tend to cause the inductor current to rise. When the transistor is OFF, the current will continue flowing through the inductor but now flowing through the diode. We initially assume that the current through the inductor does not reach zero, thus the voltage at V_x will now be only the voltage across the conducting diode during the full OFF time. The average voltage at V_x will depend on the average ON time of the transistor provided the inductor current is continuous [2].

3.1. Transition between continuous and discontinuous

When the current in the inductor L remains always positive then either the transistor $T1$ or the diode $D1$ must be conducting. For continuous conduction the voltage V_x is either V_in or 0. If the inductor current ever

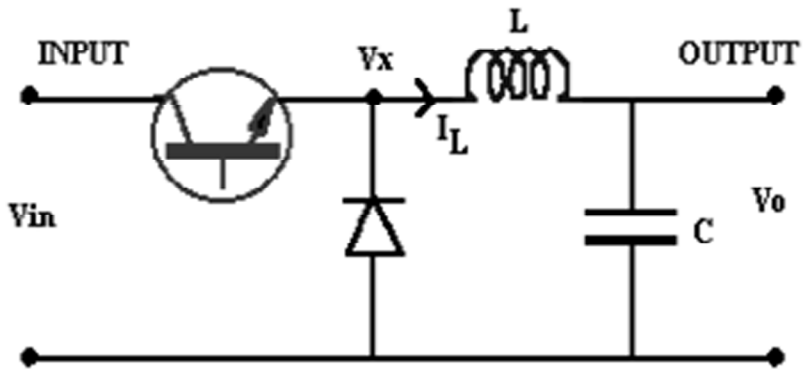

Figure 5: Buck Converter

goes to zero then the output voltage will not be forced to either of these conditions. At this transition point the current just reaches zero as seen in Fig. 6. During the ON time V_{in}-V_{out} is across the inductor.

3.2. Full-bridge or "H-bridge" Voltage Source Inverter

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Fig.7. The inverter circuit consists of four main switches and four freewheeling diodes.

3.3. Gate Signal and Inverter Operation

According to four-switch combination, three output voltage levels, $+V$,$-V$, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 7 switch of S_1 and S_4 are closed at the same time to provide V_AB as a positive value and a current path for I_o. Switch S_2 and S_4 are turned on to provide V_AB a negative value with a path for I_o. Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes. In case of zero level, there are two possible switching patterns to synthesize zero level for example 1) S_1 and S_2 on, S_3 and S_4 off, and 2) S_1 and S_2 off and S_3 and S_4on. A simple gate signal, repeated zero-level patterns, is shown in Fig. 8. All zero levels are generated by turning on S_1 and S_2.

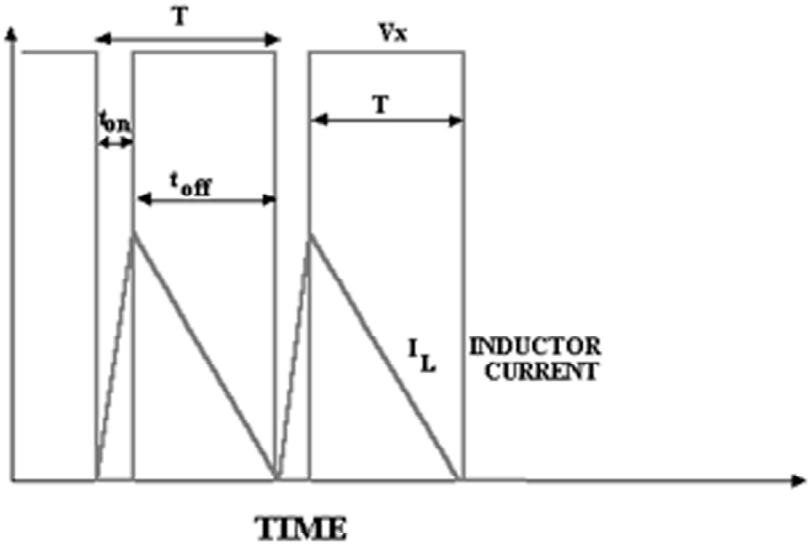

Figure 6: Buck Converter at Boundary

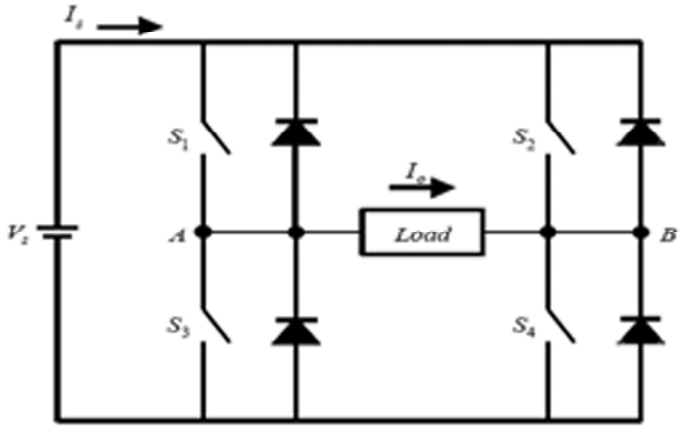

Figure 7: H-bridge cell

3.4. Repeated zero-level switching pattern

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Fig. 9 S_1 and S_2 are turned on longer than S_3 and S_4 do in each cycle because the same zero level switching pattern is used. As a result, S_1 and S_2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero stage S_1 and S_2 are turned on then in the second zero stage S_3 and S_4 are turned on instead of S_1 and S_2. By applying this method turn-on time for each switch turns out to be equal as shown in Fig. 10. This switching pattern will be used for experimental verification in this paper.

3.5. Blanking Time

Another issue that has to be concerned is providing blanking time for gate signal. The switches were assumed to be ideal, which allowed the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In practice, switching devices are not ideal [5]. To completely turn-off the devices a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time, t_D, which is conservatively chosen to avoid cross conduction current through the leg. A blanking time concept is illustrated in Fig. 10. The leg of S_1 and S_3 are used as an example.

4. SIMUALTION RESULTS

The circuit has been simulated using MATLAB R2013a software with Simulink toolbox. Simulink is a software package for modeling and analysing dynamic systems.

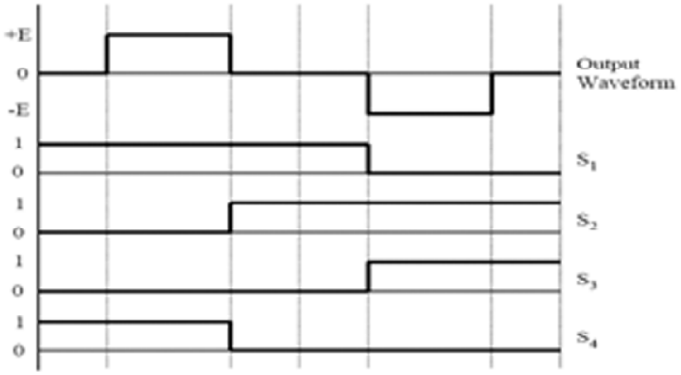

Figure 8: Gate signal pattern levels

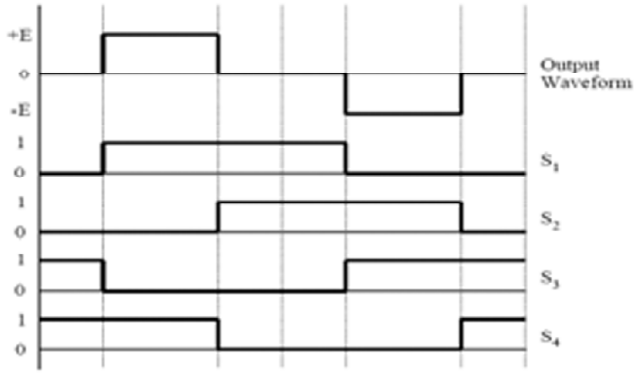

Figure 9: Swapped zero-level switching pattern

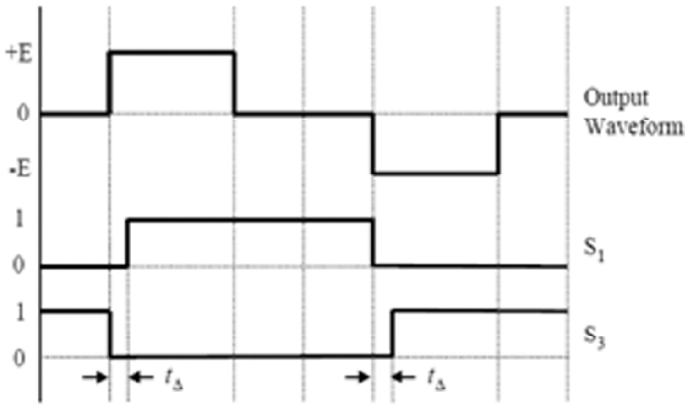

Figure 10: Apply blanking time to the gate signal

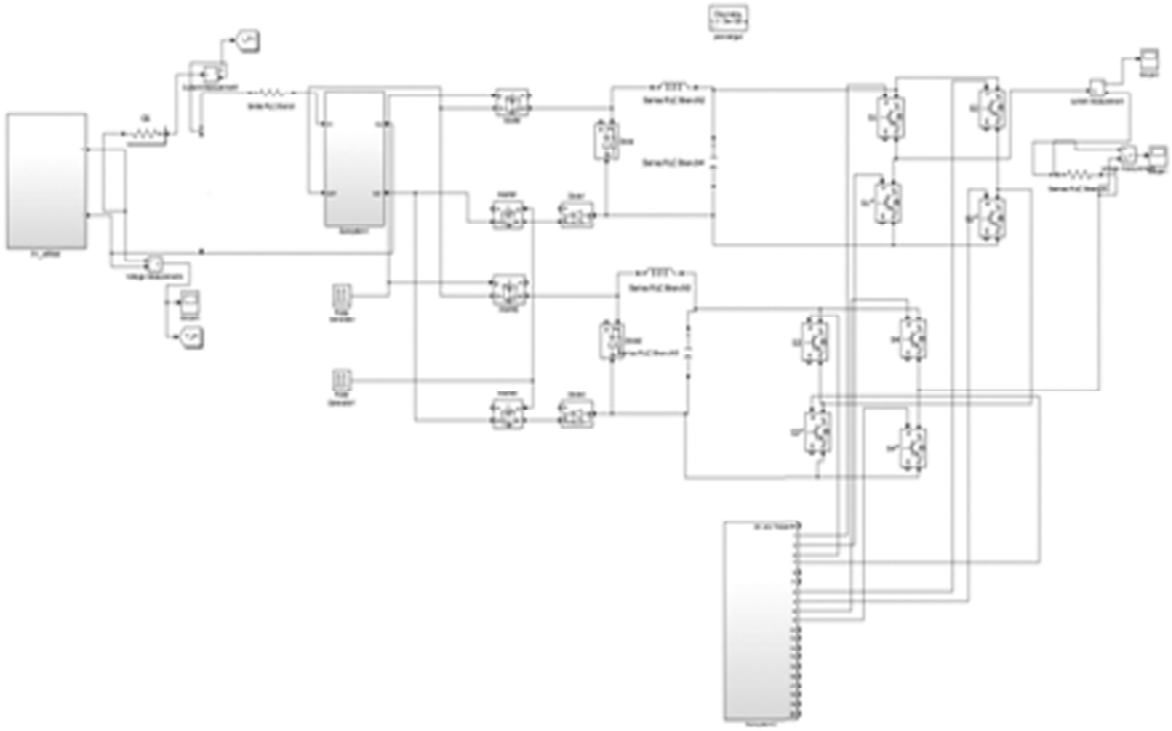

Figure 11: The simulation module of the proposed system

Here we used PV as our input source as shown in the Fig. 11. Then THD is reduced through Quasi Z-source network.Then a buck converter is used to maintain the stability according to the demand.Then multilevel h-bridge inverter is used.Herewecontrolling the inverter switch by PWM controlling technique.

Input Voltage

The below waveform in the Fig. 12 shows the input voltage from the PV input source, X axis1 div = 0.1s, Y axis 1div = 0.001V.

Output Voltage

The below waveforminthe Fig.13 shows the output voltageof the multilevel inverter, X-axis 1 div = 0.01s, Y-axis 1 div = 20V.

Output Current

The below waveform in the Fig.14 shows the output current of the multilevel inverter, X-axis 1 div = 0.05s, Y-axis 1 div = 1V.

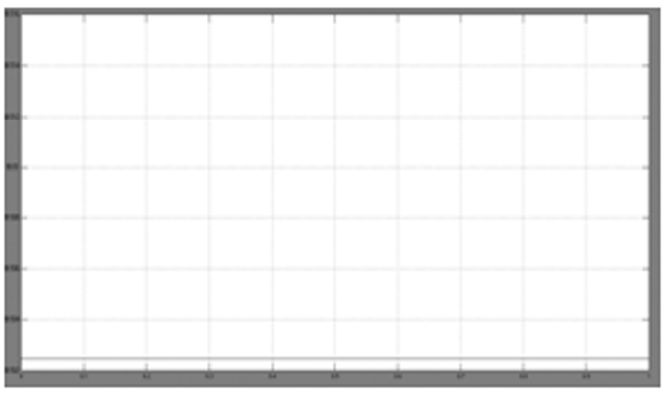

Figure 12: Input voltage from PV source

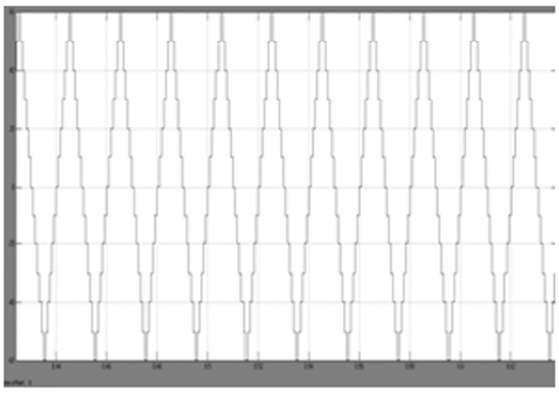

Figure 13: Output voltage of multilevel inverter

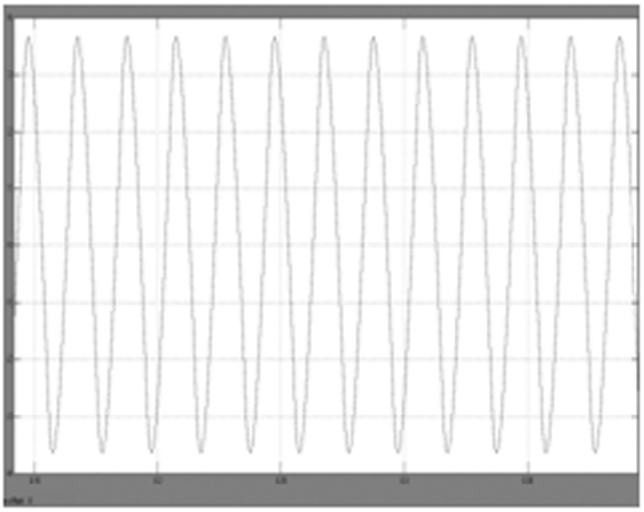

Figure 14: Output current of multilevel inverter

TOTAL HARMONIC DISTORTION OF THE SYSTEM

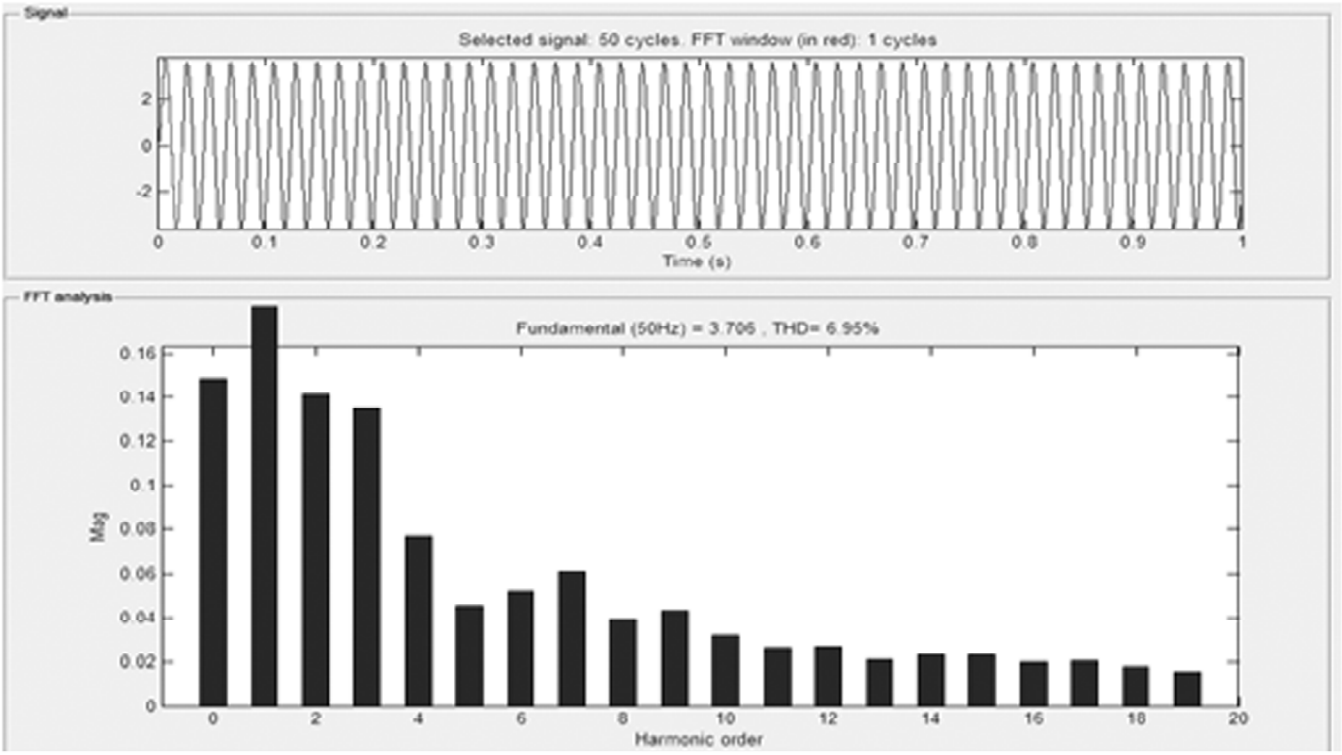

Figure 15: Harmonic distortion

In our system the total harmonic distortion is reduced much asthe analysis shown in Fig. 15.

5. CONCLUSION

This work presents a new CD-CA, 11-level topology which combines a modified DC-DC Buck Converter and hybrid Cascade converter based on two H-bridge, in single phase structure. The important advantages of the 11-level topology with QZS proposed i) Single DC source without need of transformer ii) Reduction of power switches. This topology is a competitive option suitable for efficiently integrating and controlling renewable power sources (such as PV, fuel cells and low-voltage wind) into low-medium voltage power grids and microgrids. For instance, a household application is the interconnection of PV modules, while in isolated microgrids the applications may be PV and fuel cells.

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