LOW POWER MULTIPLIER OPTIMIZED BY MODIFIED PARTIAL PRODUCT SUMMATION

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Abstract: Multiplication is a commonly used operation of Digital signal processing. The objective of a good multiplier is to provide a physically compact, high speed and a low power consuming chip. A low power multiplier using a dynamic range determination unit and a modified upper/lower left-to-right in the partial product summation is designed. The proposed multiplier is based on the modified booth algorithm and parallel operation of partial product summation which accelerates multiplication speed. Prior to executing a multiplication, effective dynamic ranges of the two input data are estimated by the dynamic range determination unit to determine that these input data with smaller and larger dynamic range are multiplier and multiplicand for booth decoding. An efficient radix-4 recoding logic generates the partial products in a left-to-right order. The partial products are split into upper and lower groups. The partial products in high precision have high chance of being zero. The upper/lower left-to-right structure is modified by moving the correction bits from upper part to lower part of partial product summation unit to reduce switching power. Additionally, low power adder cells instead of the conventional full adders are added in upper/lower parts of partial product summation to conserve power. The proposed and conventional multipliers are implemented and simulated using Modelsim, Microwind and Xilinx. The simulated results demonstrate that the proposed multiplier consumes the least power than the conventional ones.

Keywords: Low power, Modified booth algorithm, left-to-right structure.

1. INTRODUCTION

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also considerable amount of energy. While performance and area remain to be the two major design tolls, power dissipation has become a critical concern in today’s VLSI system design. Many DSP algorithms such as digital filters, adaptive filters, transforms and correlations usually employ repetitive multiplication operation. Hence, the multiplier has become a basic unit in various hardware platforms. Chen et al. developed a multiplier based on radix-4 booth algorithm with dynamic range detection to minimize switching activities of partial products, thus reduce power consumption [1]. Hsu et al. adopted a right-to-left structure of a multiplier with a tiled partial product compressor tree to minimize power dissipation [2]. In Huang et al.’s multiplier, upper/lower left-to-right structure was demonstrated to be better than the general multiplier structures [3]. Kang et al generated fewer partial products using the special two’s complement data representation to lower overall operational time and power consumption in partial product summation (PPS) [4].

In this work, a low power multiplier using a dynamic range determination unit and a modified upper/lower left-to-right (ULLR) structure in the PPS unit is designed. This multiplier adopts radix-4 booth algorithm to yield partial products. Additionally, the dynamic range determination unit is used to select one of the two input data with the smaller dynamic range to address booth decoders that generate multiple partial products based on the other input data with a larger dynamic range. Additionally, adder cells in PPS is well addressed to effectively lower power dissipation. Compared to previous work, the proposed multiplier not only modifies the upper/lower left-to-right structure but also decreases power consumption and critical delay of the partial product summation unit. The experimental results from Microwind, Modelsim and Xilinx show that the proposed multiplier is superior to conventional ones in power saving.
2. DESIGN OF PROPOSED MULTIPLIER

The design techniques such as Glitching power minimization by selective gate freezing, Fast power efficient circuit lock switch-off schemes, power-aware scalable pipelined booth multiplier, Partially Guarded Computation (PGC), High performance low power left-to-right array multiplier design are the existing works that reduce the power consumption. Glitching power minimization by selective gate freezing replaces some existing gates with functionally equivalent ones that are frozen by asserting a control signal. It can only achieve savings of 6.3% in total power dissipation. The drawbacks of Fast power efficient circuit lock switch-off scheme are the need for two independent virtual rails and two transistors for switching each cell. A power-aware scalable pipelined booth multiplier design can obtain a 20% power reduction with a 44% area overhead. Partially Guarded Computation divides the arithmetic units into two parts and turns off the unused part to minimize power consumption. It can reduce power consumption by 10% to 40% in an array multiplier with 30% to 36% area overhead. In all the above techniques there is no improvement in speed.

To reduce delay in array multipliers, certain level of parallelism is introduced in left-to-right leapfrog structure (LRLF). One approach is to split the PP bit array into even PP’s and odd PP’s. The final vectors are merged by using an adder. This algorithm is even/odd LRLF (EOLRLF). Another approach is to split the PP bit array into upper PP’s and lower PP’s. This algorithm is named upper/lower LRLF (ULLRLF). Compared with EOLRLRF, ULLRLF has two advantages. First, the shifting distance between partial products is only 2 bits instead of 4. Second, the final adder in ULLRLF is only (n+2) bit contrast to (2n-3) bit in EOLRLF [5].

Figure 1 shows the conventional and proposed multiplier architectures in which word lengths of input data X, Y are N bits. The DRD unit is allocated to determine the effective dynamic ranges of the input data. The data latches are responsible for pipelining to reduce the delay incurred in data access and computation. The partial product generation (PPG) unit, partial product summation unit and carry propagation adder are used to fulfill the arithmetic operation of multiplication.

The partial product generation unit generates the partial products of multiplication according to radix-4 booth algorithm. The PPS unit is used to accumulate the partial products from the PPG unit to yield a sum and a carry that are added by the CPA unit to produce the final product. The DRD unit can increase the chance of partial products in high precision being zero. The left-to-right summation structure in the PPS unit can lower switching activities of partial products in high precision being added and does not increase switching activities of partial product summation in low precision. Accordingly, the PPS unit based on the left-to-right structure is preferred in our low power multiplier. As compared to the conventional left-to-right multipliers, the proposed multiplier employs the modified upper/lower left-to-right structure in which low power full adders are adopted to decrease the power consumption and critical delay of PPS unit.

2.1. DRD and PPG UNIT

Multiplication consists of three steps: (1) the first step to generate the partial products; (2) the second step to add the generated partial products until the last two rows are remained; (3) the third step to compute the final multiplication results by adding the last two rows. Various multiplication algorithms such as Booth, modified Booth, Braun, Baugh-Wooley have been proposed. The modified Booth algorithm reduces the number of partial products to be generated and is known as the fastest
multiplication algorithm. This algorithm reduces the number of partial products by half in the first step [6].

The block diagram of dynamic range determination unit is depicted in Figure 2. In this figure, three bits per group are detected owing to radix-4 booth decoding [7]. The effective dynamic ranges of two input data are compared to select the input datum with the smaller dynamic range as the multiplier for booth decoding. Figure 4 shows the partial product generation unit which can reduce power consumption and glitches of the partial product summation unit.

2.2. Modified PPS Unit

In order to decrease power consumption and critical delay, the PPS unit using the modified ULLR structure, as shown in Figure 3 is adopted in the proposed 16×16 bit multiplier where the partial products PP0-PP7 are partitioned into two parts, upper and lower partial products [8] - [9].

Such partitions can allow parallel summation of these two parts to reduce the delay of the PPS unit with an upper/lower left-to-right structure. In the conventional left-to-right summation, the summation in the lower part of PPS unit usually consumes more power than the summation in the upper part of PPS unit because of the glitch effect accumulated from the upper part. To minimize the glitch effect, when upper and lower parts of PPS unit are individually added in parallel, the power consumed from the transient states can be reduced. Figure 5(a) and (b) depicts the proposed summations of the upper and lower structures, respectively, which are implemented by many full adders (FA) and half adders. The correction bits associated with sign extension (SE) are added in the lower part of the proposed PPS whereas they are added in the upper part of the conventional PPS.

3. RESULTS AND DISCUSSION

For a 16 × 16 multiplier, the result obtained from the PPG unit is of 17 bits. The sum and the carry bits obtained from the partial product summation unit are added in the carry propagate adder unit to yield the product of multiplier and the multiplicand. The full adders used in the above structure are composed of 24 transistors. Instead of the conventional ones, full adders composed of 12 transistors are used in the upper/lower structure to reduce cost and area.
developed. By using modelsim and microwind, the proposed multiplier is implemented and demonstrated to have least power consumption and least product of area, delay and power consumption than the conventional multipliers. Since the multiplier makes use of parallel operation in the partial product summation unit, the computational speed of the multiplier is higher than the conventional multipliers. Therefore the proposed multiplier can be a good candidate to achieve low power computations for various multimedia applications.

REFERENCES


